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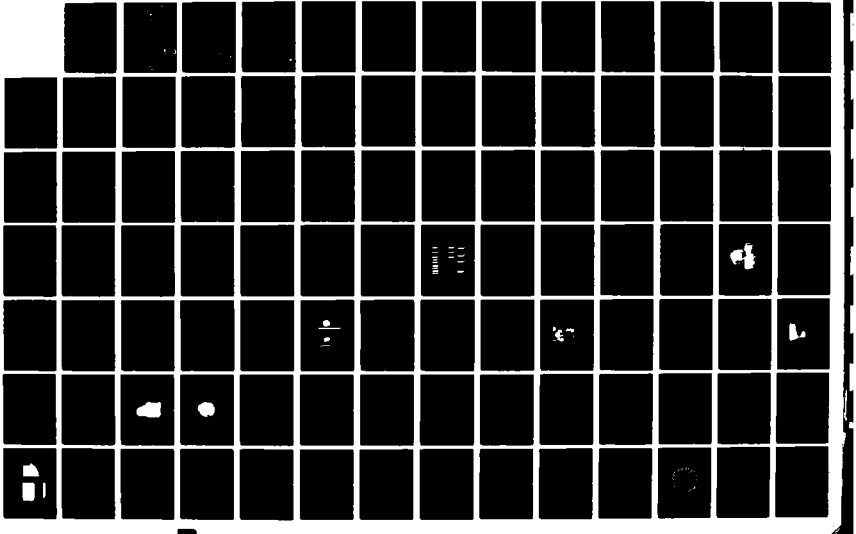

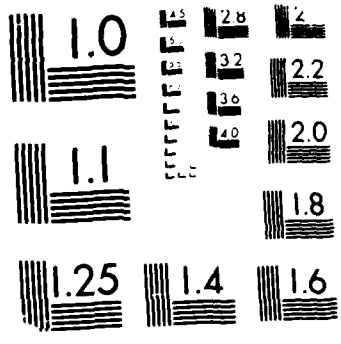

INVESTIGATION OF A HYBRID WAFER SCALE INTEGRATION TECHNIQUE THAT MOUNTS DISCRETE INTEGRATED CIRCUIT DIE IN A SILICON SUBSTRATE

THESIS

Robert W. Mainger, Captain, USAF

AFIT/GE/ENG/88M-7

DEPARTMENT OF THE AIR FORCE

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AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

Robert W. Mainger, B.S.E.E., B.A.

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Preface

This project is unique in that the research and writing portions were completed as a part-time student while I was assigned at the Foreign Technology Division (FTD). It is one of the few master's theses completed at the Air Force Institute of Technology by an Air Force officer in a part-time student status. Without the cooperation of many individuals at FTD, this research project would never have been accomplished. I give my sincere thanks to Colonel James Holt, Major Gerry O'Connor, and Mr. Thomas Antonelli for their continued support throughout this research. My thanks also go to my colleagues in the Advanced Research Branch for filling in for me during my weeks at the laboratory.

Many thanks to my thesis advisor, Major Edward Kolesar, for his support, advice, and patience. His many reviews of the drafts were invaluable. Likewise, my thanks go to the readers on my thesis commitee, Colonel James Holt, Major Donald Kitchen and Captain Richard Linderman. While conducting my research, Mr. Don Smith gave many hours of his time, for which I am grateful.

My deepest thanks go to the joys of my life, my wife, Leslie and my children, Christina, Tabitha, Joseph, and Heather who continually supported me with their love, understanding, patience, and prayer. To them, I dedicate this project.

Finally, I praise and thank God for His daily grace and strength, provided to me, without which I would never have persevered.

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[illegible] substrate [illegible] the gap between the die and the [illegible] applying a [illegible] dielectric smoothing layer, and then [illegible] the die utilizing a thin-film metallization conductor [illegible]. The study establishes a fabrication process by which the [illegible] circuit die can be close-mounted and reliably interconnected with relatively low loss [illegible].

The study is composed of four phases. The first phase is the Wet Orientation Directed Etching (WODE) study which investigated the suitability of two silicon orientations and three etchants for creating the die "wells" in the support substrate. The second phase was the Die Attach Adhesive (DAA) study which investigated the performance of several hybrid circuit attachment adhesives for mounting the die in the "wells" of the substrate. The third phase involved the preparation of final samples for electrical performance evaluation. This phase utilized the results of the first two phases and involved a series of minor experiments which determined the optimum combinations of materials, techniques, and processing temperatures critical for achieving the final product. In the fourth phase, the evaluation of the electrical and thermal performance of the WSI samples was accomplished. In addition, the functional circuits were subjected to 60-hour, mean-time-to failure (MTTF) electrical tests at room temperature and 150 degrees Celsius. The

surviving samples were then subjected to high temperature tests up to 350 degrees Celsius. After failure, each circuit was inspected to locate the failure. The early mortality percentage of the 54 circuits tested was 29.6%. Three failures occurred after 60-hour tests at room temperature (5.6%); and three failures after the 60-hour test at 150 degrees Celsius (5.6%). Five of the remaining 40 circuits (9.3%) failed when ramped to 350 degrees Celsius. Overall, 25 of 54 circuits (46.3%) survived all tests.

INVESTIGATION OF A HYBRID WAFER SCALE INTEGRATION TECHNIQUE THAT INVOLVES MOUNTING DISCRETE INTEGRATED CIRCUIT DIE IN A SILICON SUBSTRATE

I. Introduction

Background

Wafer Scale Integration (WSI) is currently being investigated for increasing the density, reliability, and speed of Very Large Scale Integration (VLSI) and Very High Speed Integrated Circuit (VHSIC) systems (1:47, 2:49, 3:845). Signal processing and digital computing systems are two candidate applications which will benefit from successful research in this area. However, the capability for direct wafer scale fabrication is limited by unacceptably low yields (3:845). In an attempt to increase the system yield, research in circuit redundancy and discretionary wiring is being vigorously pursued (1:47, 2:49-53, 4:54-58, 5:339-344).

Many of the benefits of WSI, however, may be achieved by considering a hybrid approach to the problem. Likewise, the problem of low yield may be solved. In Hybrid Wafer Scale Integration (HWSI), electrically tested VLSI or VHSIC die may be close mounted utilizing several schemes, and interconnected to achieve enhanced system performance (3:845, 6:28). Various types of MOS and bipolar circuits may be combined using a wafer scale package that synergistically accommodates the flexibility and reliability of hybrid integrated circuits with the close-packing advantage of the WSI approach.

The traditional hybrid method of interconnections between circuit die has been to use wire bonds between die pads and board leads (7:6). At

high operating frequencies, parasitic impedances are significant and act to limit the switching performance of the system (7:12). It has been proposed that many of these parasitics would be eliminated if the die's top surface was mounted coplanar with the top surface of the substrate, and interconnections made by means of thin-film metallic conductors acting as microstrips (7:12).

Problem Statement

This study investigates a hybrid method of WSI which involves mounting discrete integrated circuit die into etched "wells" of a supporting wafer, aligning the top surfaces of the die and the support substrate, planarizing the gap between the die and the substrate, applying a conformal dielectric smoothing layer, and then interconnecting the circuit die using a patterned thin-film metallization technique. This study seeks to establish a fabrication process by which electrically tested integrated circuit die can be close-mounted and reliably interconnected with relatively low impedance microstrip conductors.

Scope

This research project was conducted in four phases. The first phase was initiated by identifying an appropriate etching technique to fabricate the circuit die "wells" in the surface of a relatively thick silicon wafer (15 - 18 mils or approximately 0.6 - 0.7 millimeters). This phase is known as the Wet Orientation Directed Etching (WODE) study. The second phase sought to identify an optimal die attach adhesive to reliably mount the circuits to the bottom of the "well". This investigation is referred to as the Die Attach Adhesive (DAA) study. The third phase involved the preparation of final samples for electrical perform-

ance evaluation. During this phase, several experiments were conducted to determine the optimal techniques, materials, and processing temperatures for preparing the final samples. The fourth and last phase focused on the electrical performance evaluation of the three samples fabricated in the third phase. This evaluation included both electrical and thermal tests, as well as the associated failure analysis. Detailed information on each phase is given in the following paragraphs.

The Wet Orientation Directed Etching (WODE) study investigates the suitability of two silicon orientations [(100) and (110)], and the performance of three chemical etchants known for their anisotropic etch characteristics:

1. potassium hydroxide in deionized water (DIW),
2. potassium hydroxide in DIW with an iso-propyl alcohol buffering reagent, and
3. ethylenediamine in DIW buffered with pyrocatechol.

This last etchant will henceforth be referred to as the PED etch. The performance characteristics of each etchant were investigated relative to the two silicon orientations. The parameters of interest included the etch rates of the silicon and silicon dioxide, the degree of anisotropy, the physical condition of the wells after etching, and the resulting shape of the wells compared to the initial masked pattern.

The Die Attach Adhesive (DAA) study investigates the suitability of several standard hybrid die attach adhesives to attach the circuit die to the bottom of the wells fabricated in the WODE study. Three gold eutectic materials (gold germanium, gold tin, and gold silicon) were evaluated, as well as several organic adhesives (silver-filled, single-component epoxies, a multicomponent epoxy, and a silver-filled glass).

Each adhesive was applied in a manner consistent with its particular application instructions. An initial "pop off" test was applied to reject any of the adhesives which could not withstand the prying force of approximately 150 grams. The remaining adhesives were examined (after application and cure) via cross-sectional dissection with a scanning electron microscope. The frequency and size of voids was established as the critical criteria for further rejection of additional adhesives. An optimal adhesive is recommended and was used throughout the continuance of this investigation.

After a suitable wet etching method and die bond adhesive was identified, the preparation of final samples for evaluation was initiated. Quartered 3 inch silicon wafers (18 mils thick) with a 3x2 array of 200 mil-square wells were etched to depths of approximately 9.6-9.7 mils. Square die (197 mils and 8.7 mils thick) were mounted into the wells using the adhesive identified in the DAA study. The technique used to align the top surfaces of the support substrate and the die involved the use of a two inch square glass flat (a de-emulsified photolithography mask) and a 100 gram weight. After the die were positioned in the wells, the glass flat was placed over the substrate, and the sample was positioned on the hotplate to cure the adhesive. The weight was then positioned on top of the glass flat to minimize any shift of the die. The effects of candidate processing temperatures on the stability of the adhesive, and the effect on the movement of the die out of position was studied with temperatures of 100, 125, 150, 175, 200, and 350 degrees Celsius.

Next, a candidate conformal material (Master Bond EP-34CA Special) and method of application for filling the "gap" surrounding the

integrated circuit die was investigated. This gap typically spans 3-30 mils, depending on the substrate's crystallographic orientation and etching. In order to be able to interconnect the die with metallic conductors, the gap region needs to be filled with an electrically insulating material. In addition, a photosensitive polyimide (Merck Selectilux, HTR 3-200) was applied to the top surfaces of the support substrate, gap area, and the mounted die to provide inter-level electrical isolation for subsequent levels of metallization. Cross-sectional Scanning Electron Microscope (SEM) micrographs revealed the polyimide's capability for providing a high degree of planarization. An experiment was performed to determine an optimum via exposure method. Sloping via walls were sought to ensure that the top level metallization patterns had a smooth transition into the vias and onto the bonding pads to realize a reliable electrical contact. Proximity printing techniques provided a means to obtain smooth transitions. Four proximity separations were investigated: 0, 14, 26, and 40 mils. For each proximity separation, test samples were fabricated, vias were etched, and the sample was subsequently metallized. After the metal was patterned into individual conductors, each via was tested for electrical continuity to the underlying aluminum pad. A simple statistical analysis of the results revealed the optimal proximity printing separation.

Standard metallization techniques were used to provide the electrical interconnections on the top surface of the samples. An experiment was conducted to determine whether using positive versus negative photoresist facilitates the aluminum etch. The effect of annealing the aluminum was also investigated. For the preparation of final samples, aluminum was evaporated to thicknesses of approximately 2.2 microns, annealed,

patterned with positive photoresist, and etched in a high-resolution aluminum etchant.

Using the samples prepared in the prior phase, electrical, thermal, and failure analyses were conducted. Each sample possessed eighteen test circuits; three on each die, and six die in each wafer substrate. Each test circuit consisted of two bonding pads and conductors, two conductors transitioning the gaps on either side of the die, two vias, and the metal conductor on the die's surface. These portions of the samples are illustrated in Figure 1-1. Initially, several premature failures were identified. The surviving functional devices were subjected to 60-hour mean-time-to-failure (MTTF) electrical tests at room temperature and 150 degrees Celsius. Current was pulsed through each circuit at a 1 kHz rate with a peak current of approximately 50 milliamperes. Digital counters were used to determine the exact time of a circuit's failure. Thermal tests were conducted to determine the effects of heat on the samples. In the first thermal test, one of the samples was placed on a 350 degrees Celsius hot plate to observe the effect of a rapid heating on the polyimide insulator layer and the aluminum interconnects. In the second thermal test, another sample was heated from 175 degrees to 350 degrees Celsius in 25 degree Celsius increments to observe the effects of a gradual heating program. Finally, that same wafer was allowed to remain at 350 degrees Celsius for 16 hours to determine the effects of extended exposure to a relatively high temperature. After the thermal tests, each failed circuit was probed to determine the exact location of its failure. The location of each failure was then identified and documented with SEM photography.

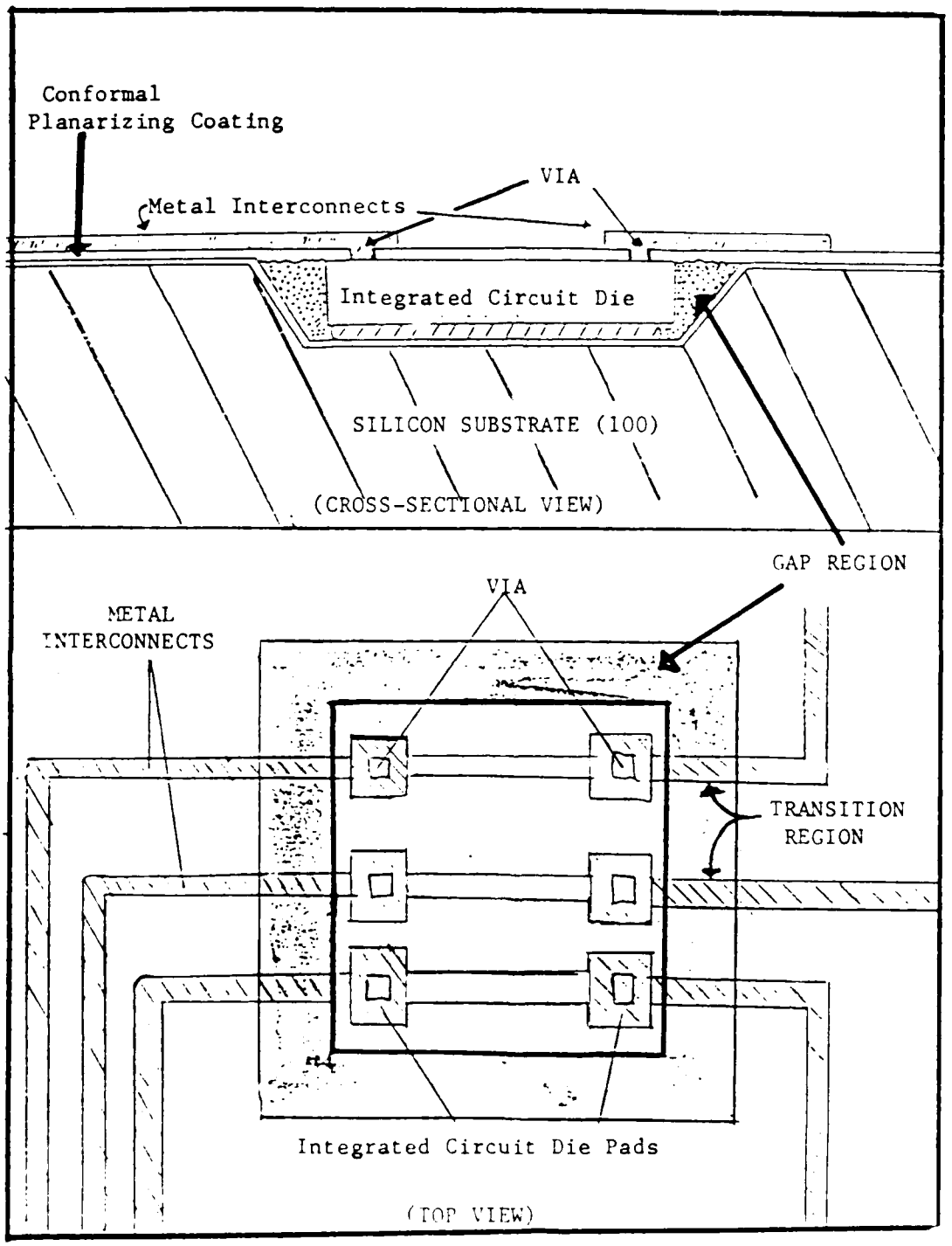


Figure 1-1. Cross-sectional and Top Views of the Die in Well. The terms used in the Scope section of Chapter 1 are illustrated.

An analysis of the advantages and disadvantages of the materials and techniques used in this initial HWSI study motivated several conclusions and recommendations concerning follow-on work, which are presented in the final sections of this paper.

Approach

This research project represents a pioneering effort at the Air Force Institute of Technology to accomplish hybrid wafer scale integration. Although the scope of this work included the actual fabrication and performance evaluation of samples, the primary focus of interest was to concentrate on the wet anisotropic etching of the well structures and the identification of the optimal die attach adhesive. The knowledge gained in these two major studies will establish the foundation for future research. The fabrication and performance evaluation of samples facilitated the operational evaluation of the choices made in the WODE and DAA studies, as well as the determination of the recommended procedures for follow-on research.

Sequence of Presentation

This thesis report is divided into five chapters, the first being this Introduction. Following the Introduction, a chapter titled "Background" is provided to acquaint the reader with detailed background information concerning the characteristics of hybrid wafer scale integration and the materials evaluated in the study. First, a review of the advantages of a hybrid approach to wafer scale integration is given, followed by a brief review of two HWSI approaches currently being researched. Second, the etch characteristics of two silicon crystal orientations and three anisotropic etchants are reviewed. Third, the

characteristics of the die attach adhesives used in the DAA study are examined. Fourth, a discussion is presented of the suitable characteristics of photosensitive polyimides for use in the project as a planarizing, inter-metal, insulating layer.

The third chapter is titled "Experimental Procedure". This chapter provides the details of the materials, equipment, and procedures implemented to realize hybrid wafer scale integration. Subsections explain the experiments used to select the optimal silicon crystal orientation and etchant for the HWSI process, identification of the optimal die attach adhesive, preparation of the final samples, and the electrical and thermal evaluation of the samples.

The fourth chapter is titled "Results". In this chapter, the results of the experiments are presented and analyzed.

The final chapter is titled "Conclusions and Recommendations". It presents conclusions drawn from the results of the experimental procedures. Recommendations for further research are also given.

II. Background

This chapter provides background information on wafer scale integration and two current hybrid wafer scale integration projects. Since this project's approach relies on anisotropic etching of silicon, a discussion concerning crystal structure and direction oriented etching is provided. Further, information on the die attach adhesives utilized is provided, as well as a discussion of the need for a polyimide inter-metal insulator layer.

Wafer Scale Integration.

Microcircuit technology has been rapidly advancing towards increasing circuit complexity, short access times, and fast clock rates, along with smaller device geometries and lower power requirements (8:509). Consequently, there has been increased research in microelectronic packaging to match the performance improvements on the chip level. One area of current research interest is Wafer Scale Integration (WSI). The goal of WSI is to integrate a number of VLSI and VHSIC die either in or on a silicon wafer to realize the revolutionary integrated circuits. Monolithic WSI uses redundant copies of a certain chip function integrated (using industry standard fabrication means) into a wafer. Instead of the wafer being diced into discrete chips, the entire wafer is further processed. Non-functional areas on the wafer are identified through electrical test. Next, using computer aided design (CAD) tools, a discretionary wiring scheme is generated that avoids these areas. Using multilevel metallization techniques, functional circuits on the wafer are interconnected. Using this technique, large parallel processor computers

with large memory areas or large signal processing systems can be integrated onto a single wafer, thus saving power, delay between circuits, and packaging costs (8:510, 9:38-39).

In Hybrid Wafer Scale Integration (HWSI), electrically tested VLSI or VHSIC integrated circuit die are close-mounted utilizing several schemes and interconnected to achieve a greatly enhanced system performance as in WSI (3:845, 6:28). Various types of MOS and bipolar circuits may be combined using a wafer scale package that synergistically accomodates the flexibility and reliability of hybrid integrated circuits (IC) with the closepacking advantage of the WSI approach. In silicon-on-silicon hybrid wafer scale integration, the silicon substrate which carries interconnects fabricated with well established IC-processing techniques, can readily accomodate 10-to-25 micron wide conductors, compared with the 3-mil conductors of the most advanced PC boards or ceramic hybrids (1:47). This conductor scaling feature helps reduce the area of a circuit to as little as one tenth of what it would be on standard printed circuit boards or hybrids (1:47). With its short wiring runs, the silicon substrate reduces parasitic inductance and capacitance by a factor of at least five (1:47). With lower impedances, the performance of the system is enhanced. Another advantage of a silicon-on-silicon HWSI approach is that the thermal coefficient of expansion of the substrate matches that of the integrated circuit, compared to the silicon-to-alumina mismatch in a conventional ceramic hybrid (1:47). This feature results in a higher packaging reliability, and thus, longer circuit life (1:47).

Two Additional Approaches to Silicon-On-Silicon HWSI.

Two silicon-on-silicon HWSI approaches were found in the literature. A synopsis of the two projects is presented below.

Auburn University HWSI. The technique investigated by Auburn University and sponsored by the Semiconductor Research Corporation is very similar to this thesis approach, with one notable difference (3:845-851). The goal is the same: to mount discrete VLSI die coplanar with a support substrate containing interconnect circuitry. The technique has wells anisotropically etched into silicon (100) orientation wafers, and these wells are etched completely through to the backside. The die are placed into the wells with their top surfaces facing downward. Thus, the top surfaces of the die are aligned coplanar with the "backside" of the etched substrate. The etched wells are preplanned in size such that the gap surrounding the die's top surface is minimized (to within a few mils). Once the die are freely mounted with an epoxy applied from the top surface, the substrate is flipped over and the former backside becomes the top surface for continued processing. A dielectric polyimide coating is spun-on and cured. Multilevel electrical interconnections are now possible (3:845-851).

General Electric HWSI Approach. In work sponsored by the United States Air Force, the General Electric Company has produced working prototypes of a hybrid wafer scale integration process known as the High Density Interconnect Hybrid Assembly (8:510). The GE approach is a silicon-on-silicon hybrid technology where fully tested integrated circuits are bonded to a flat, polished polysilicon substrate (alumina substrates have also been investigated). A "frame", made from a proprietary material, is prepared by accurately cutting wells to match the location of the die bonded to the substrate. The frame is then bonded to the substrate. Since the IC die are back-etched to a uniform thickness matching the thickness of the frame, the die's top-surfaces are

planar with the top-surface of the frame. A polyimide overlay layer is applied to provide a planarizing, dielectric coating upon which the copper metal interconnects are made through vias. A second overlay layer can then be applied giving the assembly a high interconnect density (8:511).

Silicon Wafer Etching

The first step in this HWSI investigation was to determine the most suitable silicon crystal orientation and anisotropic etchant for etching the wells into which the discrete integrated circuit die were bonded. Therefore, background information on the silicon wafers, etchants and the predicted etching results is presented in the next section. The study which investigates chemically etching large dimensional wells in a silicon substrate is referred to in this report as the Wet Orientation Dependent Etching (WODE) study. Wet chemicals were used for the etching. The rates at which the chemicals etch in a given crystallographic direction in the silicon lattice are dependent on the direction and the specific etchant (13:1185). Hence, the term "Wet Orientation Dependent Etching" is given to the process.

Silicon Wafers. Background information is provided to aid the reader in understanding the phenomena of anisotropic or orientation dependent etching. The discussion begins with the crystal structure of the silicon wafers.

Silicon Crystal Structure. Silicon (Si) in its elemental form belongs to the cubic class of crystals. When processed into the simple crystal form, it has the diamond crystal lattice. The diamond lattice consists of two interpenetrating face-centered cubic (f.c.c.)

sublattices, with a corner atom of the second sublattice located at one fourth of the distance along an internal diagonal of the first sublattice (10:3). The diamond lattice is illustrated in Figure 2-1. Directions in crystals belonging to the cubic class, such as silicon, can be conveniently described by the Miller index notation system. With respect to the rectangular (cartesian) coordinate system, any plane in space can be described by the equation (10:8):

$$\frac{x}{a} + \frac{y}{b} + \frac{z}{c} = 1 \qquad (2\text{-}1)$$

where a, b, and c represent the intercepts made by the plane on the x, y, and z axes, respectively. Writing h, k, and l as the corresponding reciprocals of a, b, and c, the equation of the plane can be equivalently expressed as (10:8):

$$hx + ky + lz = 1 \quad . \qquad (2\text{-}2)$$

In the Miller index notation, any plane (cartesian coordinate system) can be expressed as (hkl). Integral values of h, k, and l are chosen (by convention) and expressed as multiples of the unit cell's crystal lattice constant (10:8). Typically, the physical and electronic characteristics of a whole series of equivalent planes within a material's crystal structure are identical, and thus, this entire family of planes can be expressed as {hkl}. Directions can also be expressed by Miller notation. A singular direction within a plane can be expressed as [hkl] and a family of equivalent directions as <hkl>. In both cases, these directions are normal to the corresponding plane (hkl) or the family of planes {hkl} in the cubic class of lattices.

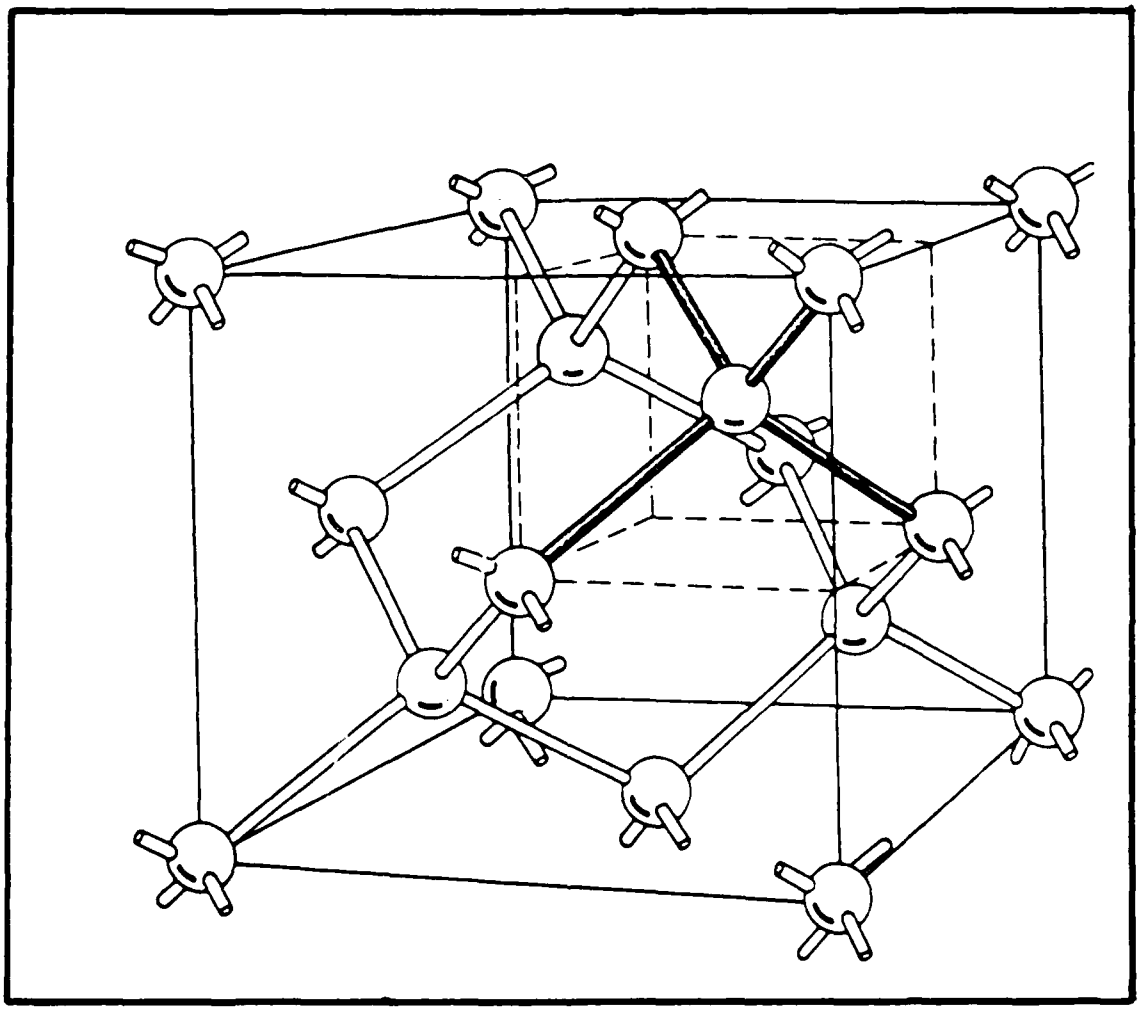


Figure 2-1. The Diamond Lattice Structure (10:7).

Planes within the silicon crystal structure (diamond lattice) can be easily identified using the Miller index notation. The families of planes which are most commonly referred to in silicon are the {100}, {110}, and {111} planes. These families of planes are commonly referenced by the (100), (110), and (111) single plane notation. In this report, the different crystal planes in the silicon materials used will be referred to by the (hkl) notation. For example, (100) silicon wafers are used. The (100) designation refers to the plane of the polished surface of the wafer; the plane corresponding to this polished surface is actually one of the {100} family of planes. The three common processing planes for silicon are shown in Figure 2-2.

Orientation Effects. Crystalline silicon has different physical and electrical characteristics with differing orientations due to the spacing of atoms in the lattice. These characteristics are discussed below.

(100) Orientation. High-quality Si wafers of (100) orientation, accurately oriented to within ± 1 degree of their crystal axes, are commercially available in a wide range of diameters, thicknesses, surface finishes, dopant types, and resistivities (12:1179). Normally, the primary flat on a (100) wafer is one of the {110} planes. Therefore, scribing or etching along directions perpendicular or parallel to the flat coincide with the location of the {111} planes. Scribing or etching along these directions are found to be very smooth, but have the tendency to form an angle of 54-55 degrees with respect to the surface. Details of why this occurs are given in Appendix A. When viewing the silicon lattice in the <100> directions, it is observed that the density of atoms is less than in the <111> direction, but much more than in the

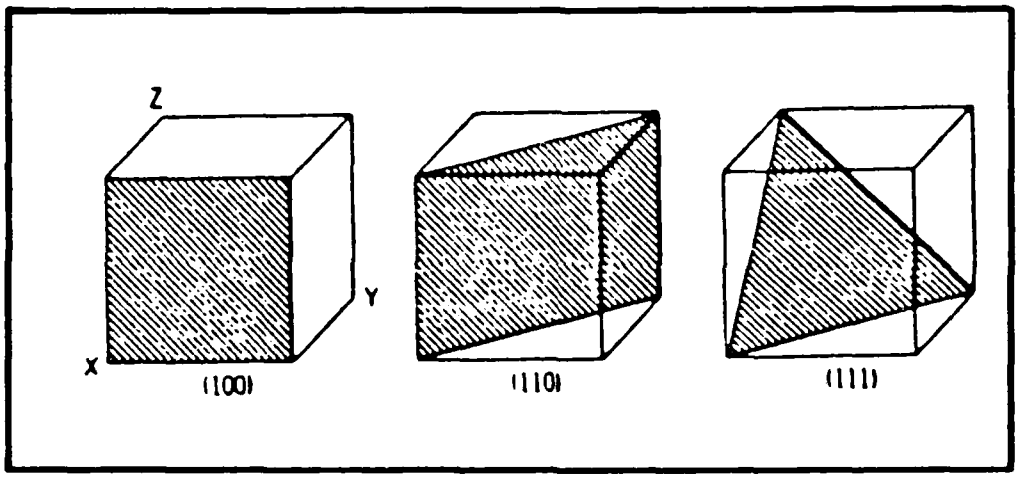


Figure 2-2. The Cubic Lattice (100), (110), and (111) Planes (11:7).

<110> direction. Further, the closest packing of atoms (shortest distance between planes) is observed in the <111> direction. The <100> direction has the second highest density, and the <110> direction has the smallest density. As a result, the following facts are observed in silicon growth and etching: the {111} planes grow and etch slowest because of their high atomic density, the {100} planes grow and etch much faster, and the {110} planes grow and etch the fastest.

The effects of anisotropically etching (100) silicon are shown in Figure 2-3. The square oxide window produces a rectangular shape as the etchant finds the nearest {111} plane and begins to etch laterally. The sidewalls theoretically form at an angle of 54.74 degrees (with respect to the top surface) (10:11). If the mask is properly aligned, such that the rectangular shapes on the mask (for example, the well shapes used in this study) are parallel to within one degree of the wafer flat, straight, rectangular shapes are formed (12:1180).

(110) Orientation. As discussed above, the {110} planes have the largest distance between planes and the smallest density of atoms per unit area. Thus, the {110} planes etch the fastest of the three primary orientations. Furthermore, wafers with the {110} orientation are often of questionable quality and are not readily available due to their limited use in industry (12:1179). The primary flat is typically one of the {111} planes.

The effects of anisotropically etching relatively shallow depths into (110) silicon are shown in Figure 2-4. While a square oxide mask window produces straight vertical sidewalls (as viewed cross-sectionally in Figure 2-4), the shape generated in the silicon is actually a rhomboid form. The sidewalls adjacent to those which form perpendicular to the

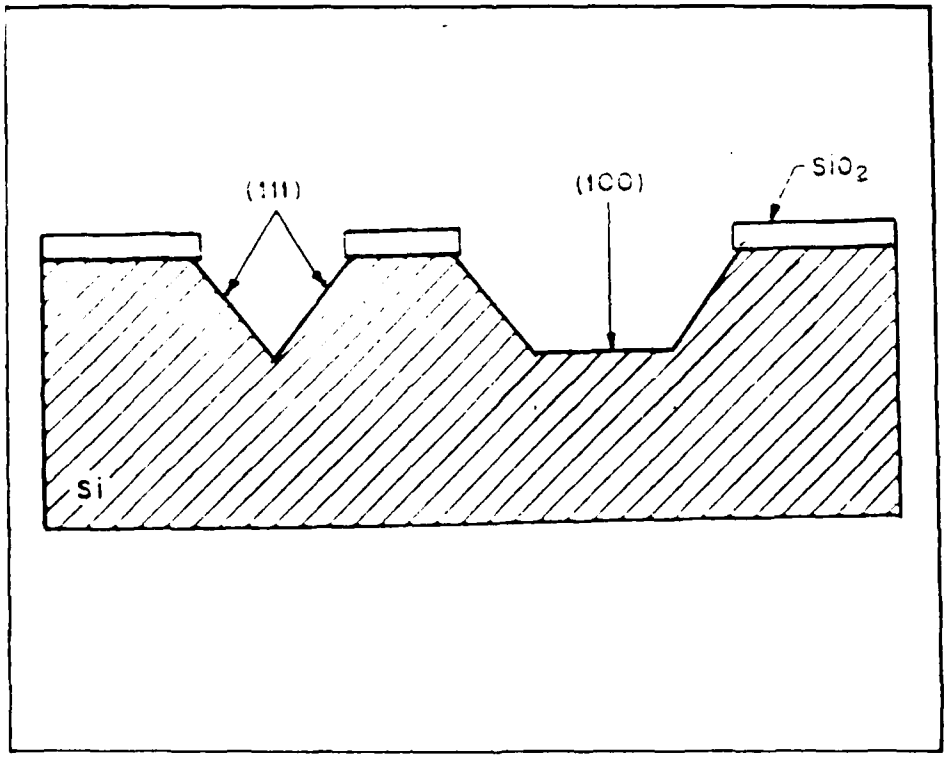


Figure 2-3. Anisotropically Etched Holes in (100) Silicon (11:456).

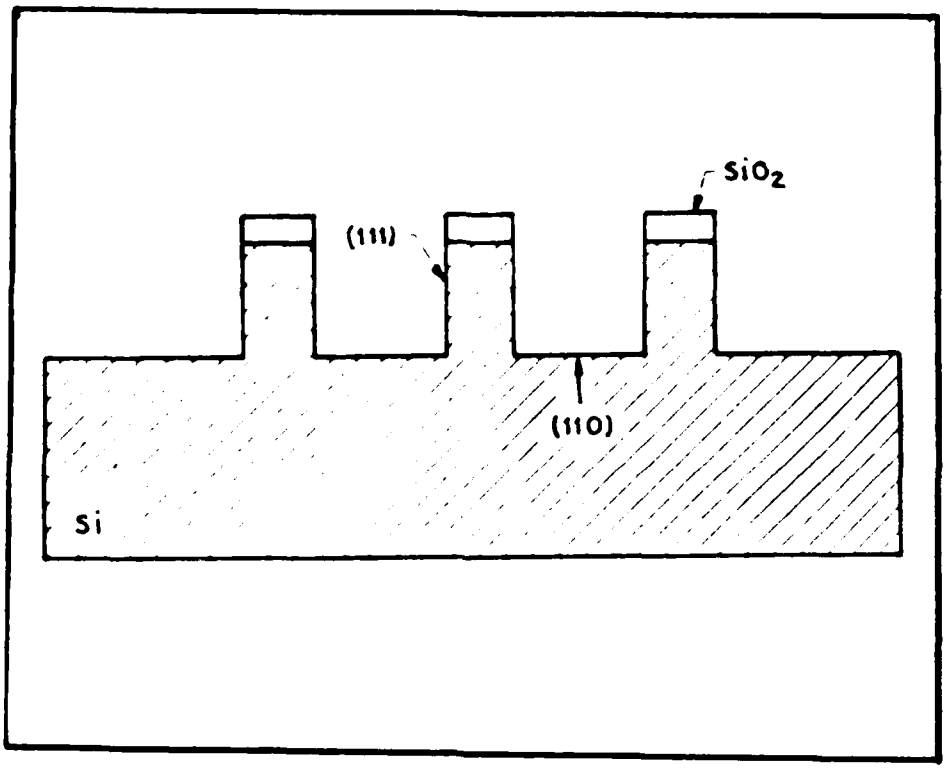


Figure 2-4. Anisotropically Etched Holes in (110) Silicon (11:456).

plane of the wafer, form sidewalls which are not perpendicular. Rather, the sidewalls form at an angle of 35 degrees with respect to the surface plane of the wafer. These results are presented by Bean (12:1179) and are from mask patterns with the dimensions on the order of 1-2 square mils and chemically etched to depths of 0.1-1.0 mils (1 mil = 25.4 microns). In contrast, this WODE study investigates the end products of etching holes on the order of ten thousand square mils and ten mils deep.

Wet Anisotropic Etchs. Anisotropic liquid etchants for silicon are usually alkaline solutions used at elevated temperatures (13:1186). The two principal reactions are the oxidation of the silicon, followed by the dissolution of the hydrated silicon. Chelation agents can be used to facilitate the dissolution process resulting in uniform and controlled etching (14:287). A chelation agent is an etchant solution additive which acts as a catalyst for breaking the silicon bonds which aides the etching process. The three wet etches used in this study are discussed in the following subsections.

Potassium Hydroxide in Deionized water Etchant. Potassium hydroxide (KOH) in deionized water (DIW) is a commonly used anisotropic wet etch. Bean, Kendall, Lee, and Weirauch recommend the use of this etchant with (110) oriented silicon (12:1186, 15:195-198, 16:4569-4574, 17:1478-1483). The prescribed composition is 1 gram of KOH per 1 milliliter of water. Since reagent grade KOH is approximately 85% by weight, the end result is a mixture which is approximately 48% by weight KOH. Bean reports that a 44% by weight mixture etches silicon up to six hundred times faster in the <110> direction than in the <111> direction when accurately (to within +0.1 degrees) aligned with respect to the (111) plane, which is typically the wafer's flat. The etch rate of

silicon is approximately 0.8 microns/minute when used at 80 degrees Celsius (13:1186). The etch rate of silicon dioxide, which is the commonly used masking material, is reported to be 30 Angstroms/minute when used at 80 degrees Celsius (13:1186).

An alternate concentration of the KOH and DIW system has been reported in the literature; the 48% by weight KOH mixture used by Kendall (15:195). This etchant has been used to etch very narrow grooves for a solar cell design (15:195). It was found that in order to obtain a 600:1 etch rate preference of the <110> direction compared the <111> direction, the mask had to be accurately aligned ($\pm$ 0.2 degrees) with the {111} plane. If accurate alignment is not achieved, the silicon etches at a slower rate and jagged edges are formed. Details of this phenomena are found in Kendall's report (15:195-197).

A proposed stoichiometric chemical reaction relationship for silicon in the KOH and DIW solution is (17:344):

$$Si + H_2O + 2KOH \rightarrow K_2SiO_3 + 2H_2. \qquad (2\text{-}3)$$

The literature does not discuss the utility of the KOH and DIW solution as the etchant for (100) silicon. Therefore, the combination of (100) silicon etched by KOH in DI water will be included in this study.

Buffered Potassium Hydroxide in Deionized Water Etchant. The buffered potassium hydroxide in the deionized water solution is a mixture of KOH, deionized water (DIW), and isopropyl alcohol (IPA). The alcohol acts as a complexing or chelating agent which aides silicon dissolution and results in a more controlled etch of both the silicon and silicon dioxide mask (16:4570). The term "buffered solution" refers to one where a chelating agent is present. Since three chemicals are present

in the solution, numerous component variations are possible. The concentration of KOH in deionized water, however, determines the alcohol's solubility. In practice, excess alcohol is added to the KOH and DIW mix. Some of this alcohol dissolves and provides the chelating feature. The undissolved alcohol floats on top of the etchant and forms a two layer mixture.

The most commonly described etchant mixture is one of approximately 20-25% by weight KOH, 60% by weight deionized water, and 15-20% by weight isopropyl alcohol. For actual mixing volumes, Bean reports a solution composed of 250 grams KOH, 200 grams of alcohol, and 800 grams of deionized water (13:1186). At this concentration, Bean obtained etch rates 100 times greater in the <100> direction compared to the <111> direction when the oxide mask is accurately aligned with respect to the (111) plane (which is parallel to the wafer's primary flat) (13:1186).

The silicon etching rate for KOH in DIW with IPA is a function of the concentration of KOH in solution and the etchant temperature. Price's study on etching with the KOH-DIW-IPA solution provides excellent data for predicting etch rates using this solution. Figure 2-5 depicts the predicted etch rate as a function of the KOH concentration with the temperature fixed at 80 degrees Celsius (18:350). Figure 2-6 shows the effect on the etch rate by varying the etchant temperature. An associated silicon dioxide (for masking) etch rate of only 28 Angstroms/minute is given (independent of temperature)(13:1186). Price also reports that the boron dopant concentration will retard the etch rate for concentrations exceeding 10^{18} boron atoms per cubic centimeter (18:342). Therefore, care must be taken to select wafer stock with non-degenerate doping levels.

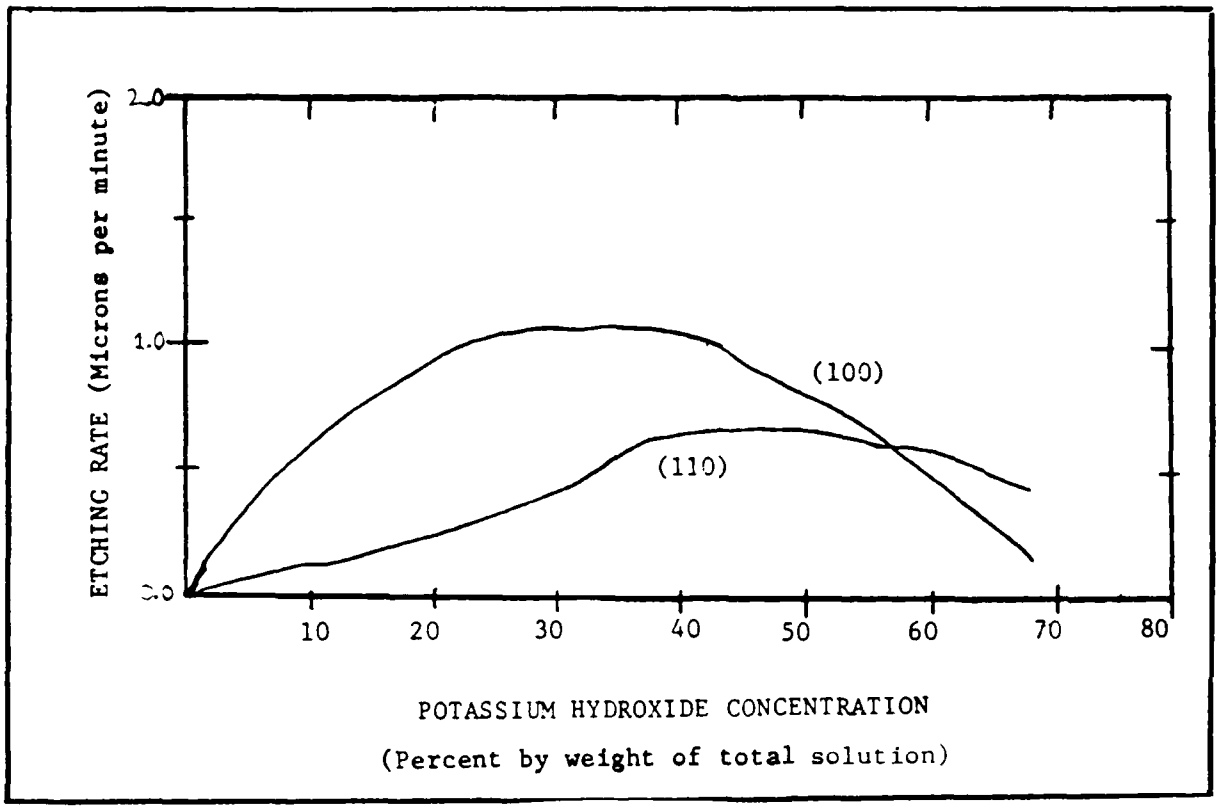


Figure 2-5. Silicon Etch Rate Versus Percentage by Weight of Potassium Hydroxide in Deionized Water With Isopropyl Alcohol (18:350).

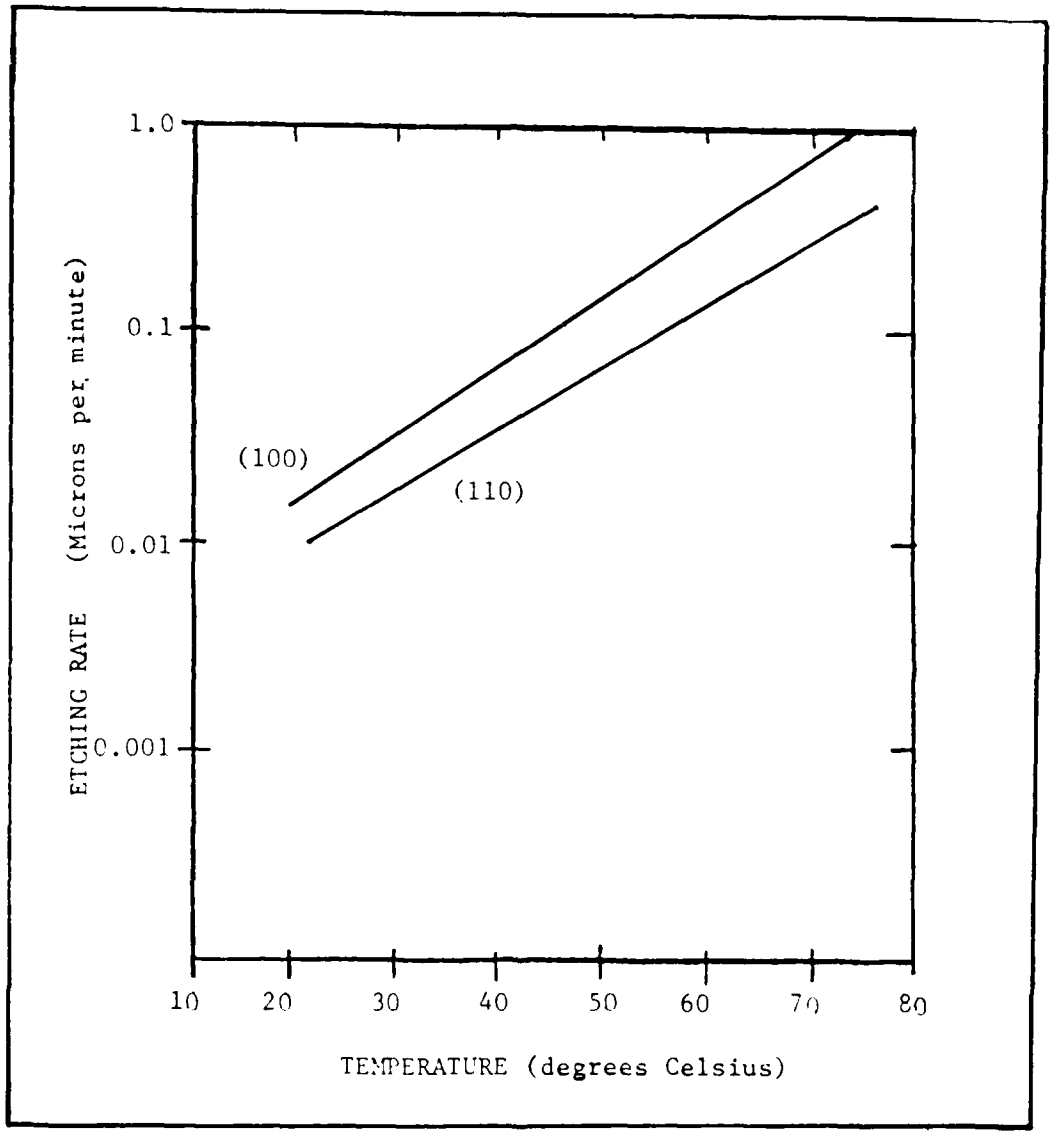


Figure 2-6. Silicon Etch Rate Versus Etchant Temperature (18:350). [Etchant: Potassium Hydroxide (25% by weight) in Deionized Water With Isopropyl Alcohol.]

A postulated stoichiometric reaction relationship for silicon in the KOH, DIW, and IPA solution is (18:344):

$$Si + H_2O + 2KOH \rightarrow K_2SiO_3 + 2H_2 \quad . \qquad (2\text{-}4)$$

Just as (100) silicon and the KOH-DIW etchant is not linked in the literature, neither are (110) silicon and the buffered KOH in water etchant. Therefore, it was also identified to be included in the WODE study.

Pyrocatechol Ethylenediamine (PED) in Deionized Water Etchant. The PED etch in water is a mixture of ethylenediamine (ED) in deionized water with pyrocatechol (P) added to act as a chelating agent (17:965). Finne and Klein studied the etching characteristics of this etchant on both (100) and (110) silicon (17:965). Again, this etchant was found to have a marked preference to etch the <100> and <110> directions compared to the <111> direction. Thus, the etch rates in both (100) and (110) silicon are quite high. In contrast, the etch rates of the silicon dioxide mask are very low.

Bean reports an etch rate of 1.1 microns/minute for (100) silicon at 100 degrees Celsius, and an oxide etch rate of 8 Angstroms/minute (13:1186). Bean also reports an etch rate of 0.8 microns/minute for (110) silicon, and a corresponding oxide rate of 30 Angstroms/minute (13:1186).

The chemical reaction in the PED etch is more complex than that associated with the KOH etches. Finne and Klein postulate the following reaction (17:967):

$$2NH_2(CH_2)_2NH_2 + Si + 3C_6H_4(OH)_2 \rightarrow 2NH_2(CH_2)_2NH_3 + [Si(C_6H_4O_2)_3] + 2H_2 \quad . \qquad (2\text{-}5)$$

The concentrations evaluated by Finne and Klein have been used frequently in other etching studies (12:1178-1185, 13:1185-1193). These concentrations are 61.2% by weight DI water, 35.1% by weight ethylene-diamine (ED), and 3.7% by weight pyrocatechol (P). In working measures, this equates to multiples of 8 milliliters DIW, 17 milliliters ED, and 3 grams of P. These rates formed the basis for preparing the solutions used in the WODE study.

Having reviewed the theory which forms the basis for the WODE study, the focus is shifted to the candidate die attach adhesives.

Die Bond Adhesives.

Critical to the success of the Wafer Scale Integration process is the choice of an appropriate die attach material. For this Hybrid Wafer Scale Integration process, the adhesive must be capable of maintaining a stable, homogeneous bond between the silicon substrate and the silicon die. There are several die bond adhesives commercially available that are appropriate for consideration in this study. A survey of these adhesives is presented.

Gold Eutectic Materials. Gold eutectic materials were used as an initial die bond adhesive and still retain a prominent position in the integrated circuit manufacturing industry (19:35). Their advantages include the fact that eutectic materials (for example, gold-germanium, gold-silicon, and gold-tin alloys) quickly solidify when reduced below their melt temperature and form a functioning bond possessing excellent electrical and heat conductivity characteristics (20:1). Eutectic materials have the advantage compared to the new generation of organic and inorganic die adhesives in that they can be easily reworked or

repaired, do not outgas at elevated temperatures, and do not retain moisture (thus, minimizing many reliability problems) (19:35-36). For these reasons, gold eutectic materials have served as the standard die bonding materials for hybrid and military standard (Mil-standard) integrated circuits.

Recently, however, the rising expense associated with gold eutectic materials, has motivated the search for alternate candidates (19:35). Additionally, there are other technical reasons why they have declined in their popularity. Specifically, these eutectic materials are not reliable for bonding larger chip sizes (greater than 250 mils on a side). The material tends to bubble and leave voids (19:35-36, 21:42). Naturally, this characteristic will be a disadvantage as die sizes continue to increase. Gold eutectic materials tend to produce a high stress bond due to the differing linear thermal coefficients of expansion (T.C.E.). Silicon fractures form when exposed to repeated thermal cycles and these result in serious reliability problems especially with respect to Very Large Scale Integrated circuits (VLSI) (19:36).

Epoxy Based Adhesives. Organic die adhesives are becoming more prominent in the microelectronics industry (22:305). Typically, an organic adhesive means an epoxy based adhesive. Three types of epoxy based adhesives are used in the Die Attach Adhesive (DAA) study presented in this thesis. Two candidates are single-component, silver-filled epoxies, and the other is a two-component epoxy. Generalized background information is provided for each of these epoxies in the following subsections.

Single-Component Silver-Filled Epoxies. Due to the expense of gold, silver-filled epoxies have become very popular in recent years

(23:38, 24:65). They are solventless blends of silver, an epoxy resin, a hardener, and a catalyst. Typically, they are pre-mixed by the manufacturer, packaged, and frozen (19:37). Users thaw the mixture at the time of each application. The shelf-life, once thawed, is approximately 1 to 5 days. One-component epoxies have an advantage because they eliminate the mixing errors associated with two-component epoxies. Typically, the one-component epoxies use "cleaner" resins than the two-component epoxies, thus eliminating many ionic contamination problems. One component epoxies have a strong advantage because they are solventless and tend to yield void-free bonds, thus increasing thermal dissipation and reducing stress (19:37).

Two-component Epoxies. Two-component epoxies or multi-component epoxies are so named because they need to be mixed to precise proportions and thoroughly mixed before use. In general, the epoxy is formed by the reaction of epichlohydrin with phenols (19:36). Silver can be mixed with one of the components to yield a conductive bond (25:200). Additional compounds can be added to obtain desirable physical and electrical characteristics. For instance, Lithium Beta-Encryptite was added to the two-component epoxy used in this study to yield an epoxy that matches the T.C.E. of silicon (26).

Inorganic Die Adhesives. Relatively new in the IC industry are the silver-glass adhesives. Silver-glasses offer excellent reliability, reduced stress (compared to the gold eutectic materials) and lower cost (19:37). The most significant disadvantage associated with the silver-glass adhesive is its process cycle. Since the adhesive is silver in a glass matrix, relatively high processing temperatures are needed to form a bond. This high temperature requirement (430 degrees Celsius is

typical) will make this adhesive difficult to use with integrated circuits and other materials which are temperature sensitive. Despite this disadvantage, users predict that by 1990, silver-glass adhesives will dominate the ceramic dual-in-line (CER-DIP) packaging which currently utilizes a 450 degree Celsius processing temperature (27:1). However, it is questionable whether this HWSI process can tolerate the need for such high processing temperatures.

Polyimides as Planarizing and Insulating Coatings.

The next critical step after bonding the die into the well structures is to coat the upper surface of the sample with a planarizing and insulating material. The next section discusses the utility of polyimides to fulfill this inter-level planarization and insulative function.

Desired Characteristics of the Insulator for the HWSI Process. To realize the needed interconnections between the integrated circuit die, inter-level insulator layers must be utilized between the metal interconnects. A common problem in every wafer scale integration scheme is to realize a reliable, low-impedance interconnect scheme between regions of the wafer (28:3128). The ideal candidate material for this function should possess the following features summarized by Saxena and Pramanik (29:97):

1. a good insulating material with low pinhole density to prevent shorting between metal layers,
2. a low dielectric constant to reduce signal delays,
3. a high modulus of elasticity to withstand thermally induced stresses (due to different thermal coefficients of expansion (T.C.E.) of the materials used),

4. good adhesion to other processing materials (to maintain monolithic integrity), and
5. a low reflow temperature to facilitate step coverage and planarization without thermally damaging the previous layers.

For this hybrid wafer scale integration process, all of the above features are needed, especially a planarization capability. Despite the choice of a particular silicon substrate orientation for the HWSI process, it is expected that a gap larger than 2 mils (or greater than 50 microns) will surround the die. The difference or delta (see Figure 2-7) between the planes of the support substrate and die surfaces can be on the order 100 microns. Therefore, the material identified as the dielectric and insulator between the layers of aluminum interconnects, must also provide a smooth, planar surface for these conductors.

Advantages of Polyimide With Respect to Other Insulators. Compared to the other commonly used insulating materials (silicon dioxide or silicon nitride), polyimide coatings provide superior results for meeting the criteria discussed above. Table 2-I lists features of each material.

The cured polyimide is found to have the lowest dielectric constant and a volume resistivity comparable to the silicon dioxide and silicon nitride. The thermal coefficients of expansion of silicon and aluminum are 5×10^{-6} and 2.5×10^{-5} $(^{o}\ C)^{-1}$, respectively (30:1). Polyimide closely matches the T.C.E. of aluminum. Its use promises minimal stress due to T.C.E. match. Polyimide also purports the lowest processing temperatures. Since the future goal of the HWSI process is to mount VLSI integrated circuits, a low processing temperature is critical. It is important that the subsequent process steps do not change the operating characteristics of the mounted ICs.

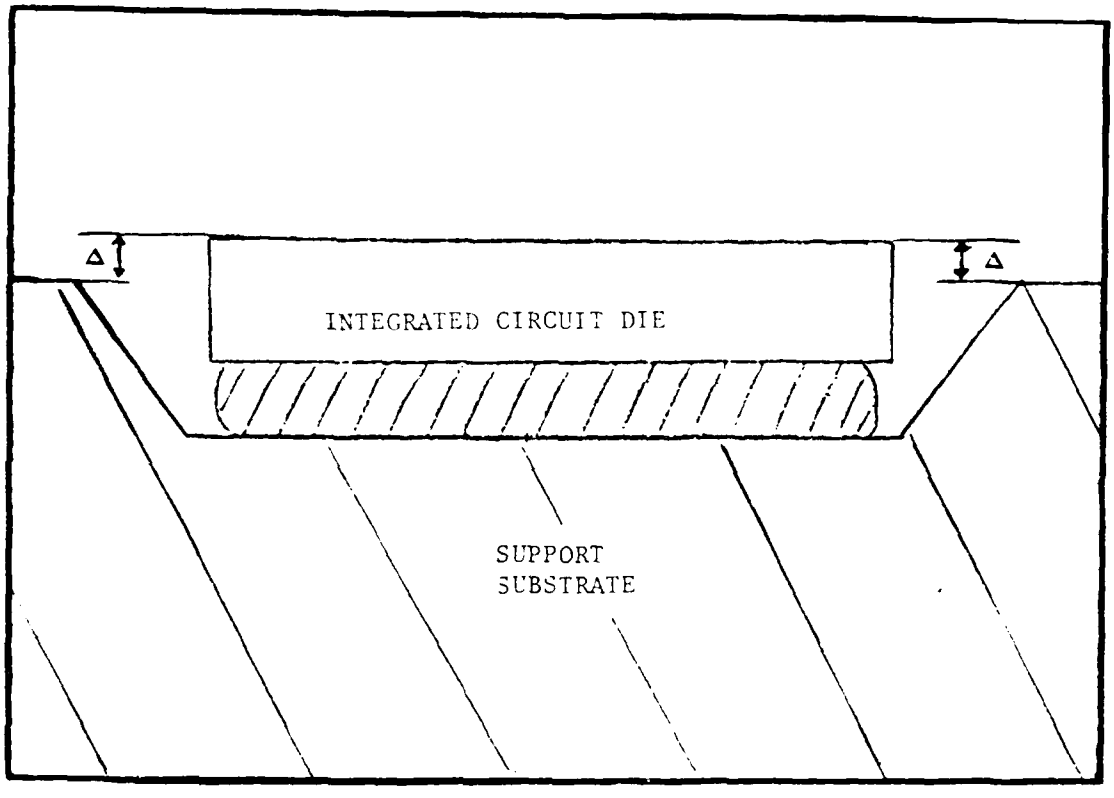


Figure 2-7. The Delta Concept Illustrated.
[The delta (Δ) is the vertical difference (in microns) between the planes parallel to the top surfaces of the support substrate and the die.]

Table 2-I. Physical Data of Polyimide and Inorganic Materials Commonly Used for Inter-level Insulation (29:1, 30:719).

		Cured Polyimide	SiO_2	Si_3N_4
Dielectric Constant	e	3.5	3.9	[illegible]
Volume Resistivity	ohm-cm	$2x10^{16}$	10^{16}	10^{18}
T.C.E.	$(^{o}C)^{-1}$	$2x10^{-5}$	$3-5x10^{-7}$	$3x10^{-6}$
Elasticity Modulus	N/mm^2	$> 2x10^{3}$	[illegible]$x10^{4}$	$2x10^{5}$
Typical Processing Temperature	^{o}C	250-450	thermal >950 CVD >450	LPCVD [illegible] PACVD [illegible]
Film Thickness	microns	1-80	0.1-3	0.1-1

CVD=Chemical Vapor deposition
LPCVD=Low Pressure CVD
PACVD=Plasma Assisted CVD

Polyimide values are representative. Specific polyimide values are for Merck Selectilux HTR 3-200.

Cured polyimide films span a wide range of selectable thicknesses (0.5 to 80 microns). This will be highly advantageous for achieving sufficient planarization. In general, the ability of a dielectric coating to planarize a surface is a function of its thickness and the step height it is planarizing (31:768). Both the silicon dioxide and silicon nitride layers are restricted to thicknesses less than a few microns. The step heights potentially planarized by the silicon dioxide and silicon nitride layers are also limited to a few microns. In contrast, polyimides can be successfully spun-on and cured to thicknesses of over 80 microns. Thus, step height differences on the same order of magnitude should be planarizable (31:777). Consequently, the utility of polyimide will be critical to the success of this research.

Advantage of Photosensitive Polyimides. Recent advances have been made in the field of photosensitive polyimides (30:1; 32:906). It is possible through the use of these polyimides, to reduce the number of processing steps for forming vias in the inter-metal insulating layer. The difference in processing is illustrated in Figure 2-8. Because of these advantages, the Merck Selectilux HTR 3-200 photosensitive polyimide was chosen for the inter-metal insulator.

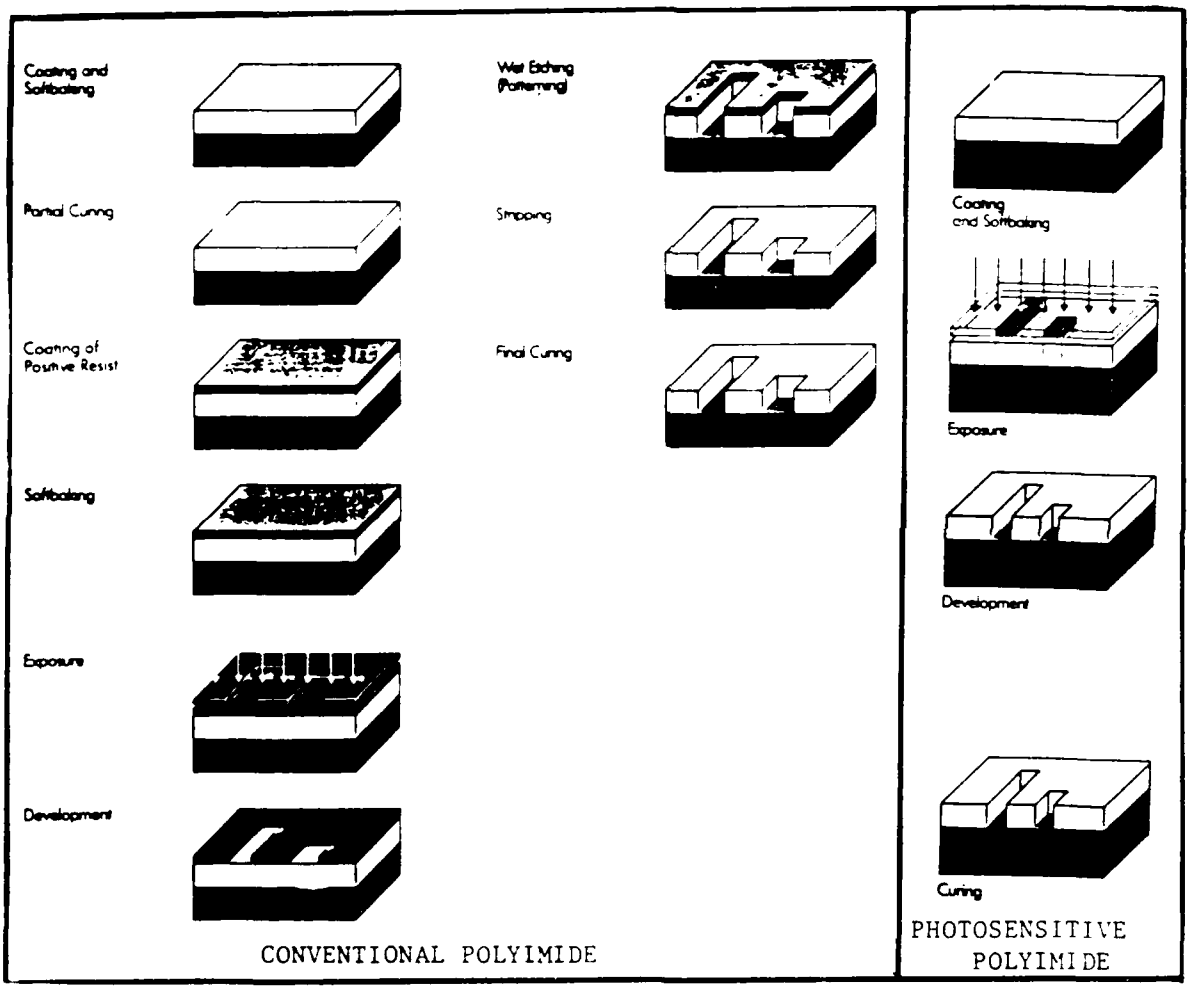


Figure 2-8. Processing Steps of a Conventional Non-Photosensitive Polyimide Versus a Photosensitive Polyimide (30:7).

III. Experimental Procedures, Equipment, and Materials

This chapter describes the experimental procedures used to accomplish this research project. As stated in the Introduction chapter, the research is divided into four phases. The first phase is a wet chemical etching study which investigates six silicon orientation and anisotropic etchant combinations. The goal of this study was to determine the optimal combination for etching the well structures into which the discrete die are mounted. The second phase of the research was a study of eight die attach adhesives and their suitability for attaching discrete die into the wells. The third phase involved the actual fabrication of final samples. Included in this phase were several experiments whose purpose was to identify optimal materials, techniques, and processing temperatures for use in the final fabrication procedure. The three final samples produced in the third phase were evaluated in the fourth phase. In this phase, various electrical and thermal tests were performed to test the durability of the samples. Fault analysis was conducted on the circuits which failed.

Many materials and instruments were used in this research project. When a material or piece of equipment is initially referenced, vendor information will be provided. Subsequent references to that same item will not include that data. Standard laboratory processes used in this project have been documented in the appendices to avoid unnecessary detail.

Wet Orientation Directed Etch Study

Information concerning the equipment, materials, and the procedures

implemented for the Wet Orientation Directed Etching (WODE) study are presented in the next section. As previously stated, the goal of this study was to investigate the suitability of six silicon wafer/anisotropic etchant combinations for etching "wells" into which discrete die can be mounted. Two orientations of silicon wafers were used in the study: (100) with both light p- and n-doping, and (110) with light n-doping (all with sheet resistivities of approximately 30 ohms /square). Three etchants were used in the study: potassium hydroxide (KOH) in deionized water, buffered KOH in deionized water (isopropyl alcohol as the buffer), and pyrocatechol ethylenediamine (PED) in deionized water. The combinations of silicon materials and etchants are summarized in a matrix in Table 3-I.

The equipment and materials used for the WODE study are not complex. Likewise, the procedures are standard processes utilized in the integrated circuit industry and are adaptable to the equipment available in the AFIT Cooperative Materials and Electronic Processing Laboratory. Photolithography masks were generated for preparing the silicon wafers for the etch process. Oxidized wafers were coated with photoresist, exposed with these masks, developed, and windows in the oxide were etched, exposing the silicon for direction oriented etching. A description of the procedure, equipment, and materials used is discussed below.

Photolithographic Masks. In order to etch wells into the surface of the support substrate, photolithography masks were needed. Appendix B describes the design equipment, materials, and procedure used to prepare the masks. The mask used in the WODE study is one containing a 2 x 3 array of 200 mil by 200 mil squares.

Table 3-I. Matrix of Silicon Wafer and Chemical Etchant Combinations.

ETCHANTS	SILICON SUBSTRATES: (100) n-and p-DOPED	SILICON SUBSTRATES: (110) n-DOPED
KOH in DIW	WODE runs #1 & 3	WODE runs #2 & 10
Buffered KOH in DIW	WODE runs # 5, 7, 8, & 9	WODE run #4
PED in DIW	WODE runs #6 & 12	WODE run #11

Key:
KOH = potassium hydroxide
DIW = deionized water
PED = pyrocatechol ethylenediamine
WODE = wet orientation dependent etching

Wafer Preparation. In order to etch precise patterns into the silicon wafers, oxide masks were formed on the surface of the support substrates. Appendix C describes the details concerning the procedure used to form these masks.

The Etching Study. The following section describes the equipment, materials, and procedure used to etch the wafers in the WODE study.

Etching Equipment and Materials. The equipment used to etch the samples evaluated in the WODE study is summarized below, and the critical components are illustrated in Figure 3-1:

1. Stainless steel vessel (10 inches high and 8 inches in diameter with a lid which supported a coiled, stainless steel tube to facilitate the passage of cooling water. The cooling water permits the lid to be cooler than the etchant, and thus, etchant in a vapor form condenses and flows back into the solution. In subsequent trials, the etchant vessel was wrapped in foil and cardboard to thermally insulate the etchant.
2. Thermometer with 1 degree graduations from 0 to 110 degrees Celsius.
3. Polypropylene wafer basket (the wafers were positioned vertically for the etching trials).
4. Hotplate with a temperature range of 0 - 500 degrees Celsius.
5. To measure well depths, a WILD optical microscope (Model CH9435; WILD Heergrugg, Ltd.; supplied by A. Daigger & Co., Chicago, IL) with magnification levels of 75x, 187x, 375x, and 750x was used.

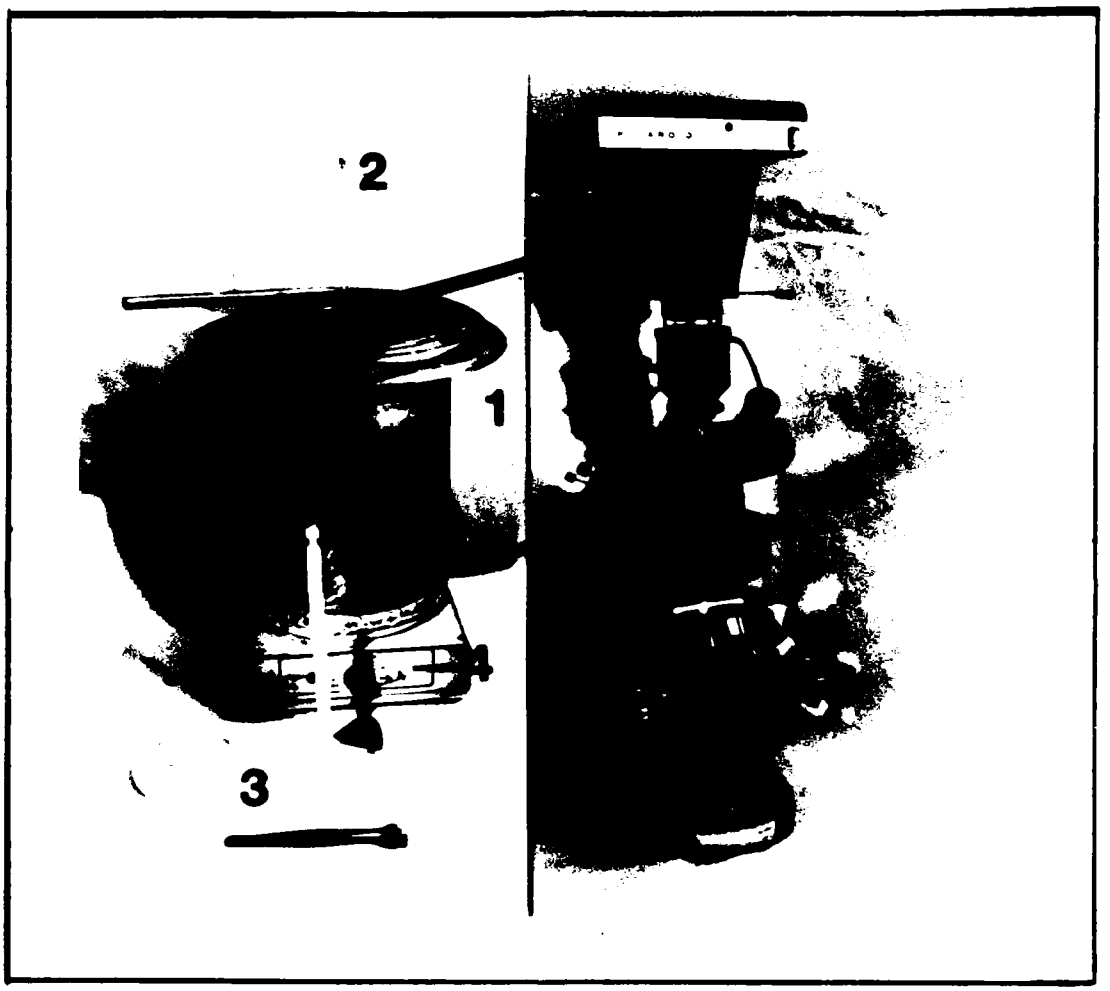


Figure 3-1. Equipment Used in the Wet Orientation Dependent Etching Study: 1) stainless steel vessel for etching with a reflux condenser cover lid (cool tap water flows through the tubing mounted on the lid), 2) Pyrex thermometer, 3) polypropylene wafer basket, 4) hot plate, and 5) WILD-Heergrugg optical microscope.

The materials used to etch the wafers are summarized below:

1. Wafers prepared according to the procedure described in Appendix C having the pattern described in the Photolithographic Masks section.

2. An anisotropic etchant, three etchants were used.

   a) 1:1 mixture of KOH and deionized water (DIW). Since reagent grade KOH is approximately 85% by weight, the etchant is approximately 45% by weight KOH in DIW.

   b) A 23% by weight KOH, 60% by weight DIW, and 17% by weight isopropyl alcohol (IPA) solution. In component weights, this solution was mixed with multiples of 230 grams KOH, 170 grams of alcohol, and 800 grams of deionized water.

   c) A 61.2% by weight DIW, 35.1% by weight ethylenediamine (ED), and 3.7% by weight pyrocatechol (P) solution. In component weights, this equates to multiples of 8 milliliters DIW, 17 milliliters ED, and 3 grams of P. 3. Tap water used for the reflux condenser cover.

The Procedure. The following procedure was used to etch the wafers:

1. The wafers were positioned vertically in the basket and confined by the basket's lid.

2. The etchant is mixed prior to use and allowed to stabilize for 24 hours. The etchant was poured in the etching vessel which was positioned on the hotplate and elevated to the desired temperature. A typical volume of etchant was approximately 1 to 1.2 liters.

3 The wafers were immersed in the etchant and the duration of immersion was recorded. A wafer was typically removed at a pre-planned period of time (for example, every 20-60 minutes). When all the wafers were removed, or when the wafers were destroyed (for example, when the well surfaces etched completely away), the run was terminated.

4. The etched features were inspected with the optical microscope at magnifications of 75X, 187X, 375X, and 750X. The observation included measuring the depth of the wells and observing the condition of the bottom of the wells. The measurement of the well's depth was accomplished by focussing on the top plane of the support substrate and noting the reading on the microscope's calibrated focussing knob. After focussing on the well's bottom plane and reading the corresponding measurement, the difference between the initial and the final readings yielded the well's depth. (Care must be taken to count the number of complete revolutions of the focussing knob, since each revolution represents 100 microns.) An average depth was determined by sampling the depths of each of the wells at different locations (typically six measurements). The well depths reported are within $\pm$ 3 microns.

The results of the study are presented in Chapter IV. The data sheets for each WODE etch trial are presented in Appendix E.

Die Attach Adhesive Study.

The following section provides information on the equipment, materials, and procedures used in the Die Attach Adhesive (DAA) study.

The intent of this study was to investigate the bonding properties of several commonly used die attach adhesives for attaching the integrated circuit die into the etched well structures. The adhesive properties of each of the materials evaluated have been previously investigated and reported by the respective manufacturers, and they are summarized in Table 3-II. The purpose of this investigation was to collect additional information concerning the suitability of these adhesives for bonding a die in an etched well.

The Materials Tested. A total of eight adhesives were investigated in the DAA study. The following section discusses each of them in detail.

Gold Eutectic Materials. Three gold eutectic alloys were tested: gold silicon (melting temperature 370 degrees Celsius), gold germanium (melting temperature 356 degrees Celsius), and gold tin (melting temperature 280 degrees Celsius). Each alloy was ordered from the Indium Corporation of America (Utica, NY) in the form of square preforms. Each preform was 190 mils square and 1.5 mils thick.

Single Component Epoxies. Two single component epoxies were tested: Amicon C-990 (Amicon Corporation, Lexington, MA) and Dynaloy SM-200 (Dynaloy, Inc. Hanover, NJ). Both are silver-filled epoxy adhesives and are electrically conductive. Amicon C-990 is 75 percent filled with pure silver, and it has a low ionic contamination level (< 10 ppm). This material is solventless, and thus, the probability of voiding is minimized (33:37). As a soft, smooth thixotropic paste it is easy to apply. The cure temperature is 150 degrees Celsius.

Dynaloy SM-200 is 75 percent pure silver filled, and it has a low ionic contaminantion level (< 10 ppm). The vendor did not provide

Table 3-II. Characteristics of the Eight Die Attach Adhesives Used in the Die Attach Adhesive Study.

Adhesive	Maximum Processing Temperature (degrees Celsius)	Adhesive Form	Resistivity (ohm·cm)	$\frac{\text{T.C.E.}_{\text{adhesive}}}{\text{T.C.E.}_{\text{silicon}}}$
AuSi	370	preform	10^{-7}	> 5
AuGe	356	preform	10^{-7}	> 5
AuSn	280	preform	10^{-7}	> 5
Amicon C-990	150	tan paste	3×10^{-4}	> 7
Dynaloy SM-200	150	silver paste	6×10^{-4}	> 7
Master Bond EP-3-CA Special	125	thick 2-part black paste	$> 10^{4}$	1
Quantum Materials QMI-2419	435	silver paste	7.5×10^{-6}	> 7

For comparison, the Thermal Coefficients of Expansion of silicon, silicon dioxide, and aluminum are given (10:254):

silicon - 5×10^{-6} (^{o}C)$^{-1}$
silicon dioxide - 2.5×10^{-6} (^{o}C)$^{-1}$
aluminum - 2.5×10^{-5} (^{o}C)$^{-1}$

information indicating the volume of solvents present in the uncured epoxy, and it is not clear what chemical differences exist between these two single component epoxies. Cure temperature of the Dynaloy adhesive is 150 degrees Celsius.

Multicomponent Epoxy. One multicomponent epoxy was tested. Master Bond EP-34CA Special (Master Bond Inc., Teaneck, NJ) is a custom formulated, two-component epoxy which has been designed, after cure, to match the thermal coefficient of expansion (T.C.E.) of silicon (2.5×10^{-6}/degree Celsius)(26). Beta Eucryptite was added by the vendor to a component of the unmixed epoxy to modify its natural T.C.E.. Beta Eucryptite is a dielectric lithium aluminum silicate (26) and is electrically nonconductive. Master Bond EP-34CA is likewise electrically nonconductive. Component A is mixed with component B in a 2:1 ratio at the time of usage and cured at 125 degrees Celsius for one hour. Outgassing of solvents is expected, and therefore, shrinkage will take place.

Silver Glass. One inorganic adhesive was tested, a silver glass, (QMI-2419, Quantum Materials, Inc., San Diego, CA) filled with 67.6 percent pure silver (electrically conductive) and considered a low ionic contaminant (< 10ppm) adhesive. The vendor's recommended processing schedule specifies a cure at a maximum temperature of 435 degrees Celsius for approximately 7 minutes.

Die Attach Adhesive Study Equipment, Materials, and Procedure. The following section describes the equipment, materials, and procedure used in each phase of the DAA study. Since there were three different processes used, the section is divided into three corresponding

sections: eutectic bonding, epoxy bonding, and silver glass bonding.

Eutectic Bonding Equipment and Materials. The equipment utilizing the eutectic bonding procedure is summarized below:

1. A heat block, machined by the AFIT Fabrication shop. The heat block is shown in Figure 3-2. It is a block of aluminum metal 1.5 inches by 1.5 inches square, and 1 inch thick. It has a raised metal plateau on the top surface with an area (0.9 inches x 0.5 inches) to match the area of the 3 x 2 well pattern. The heat block was heated on a hot plate to the desired processing temperature. A chromel alumel thermocouple was inserted into a passage within the heat block and connected to a digital temperature meter. Temperature control was achieved manually. The wafers prepared for bonding were placed on the raised area so that localized heating occurs under the area of the die to be bonded. Adjustable guides on the heat block facilitate the accurate placement of the sample.
2. A digital thermometer with a cromel alumel thermocouple (Model 101, Omega Engineering, Inc., San Jose, CA) with a 0 - 500 degree Celsius range.
3. Hot plate 0-400 degree Celsius range.
4. IC die handling tools (assorted tweezers).
5. Two inch by two inch glass photomasks and a 100 gram weight

The materials used in the eutectic bonding procedure are summarized below:

1. The three gold eutectic alloys described above.
2. Etched silicon wafers. Quartered 3-inch (100) wafers were used throughout the DAA study. They were approximately 20 mils thick.

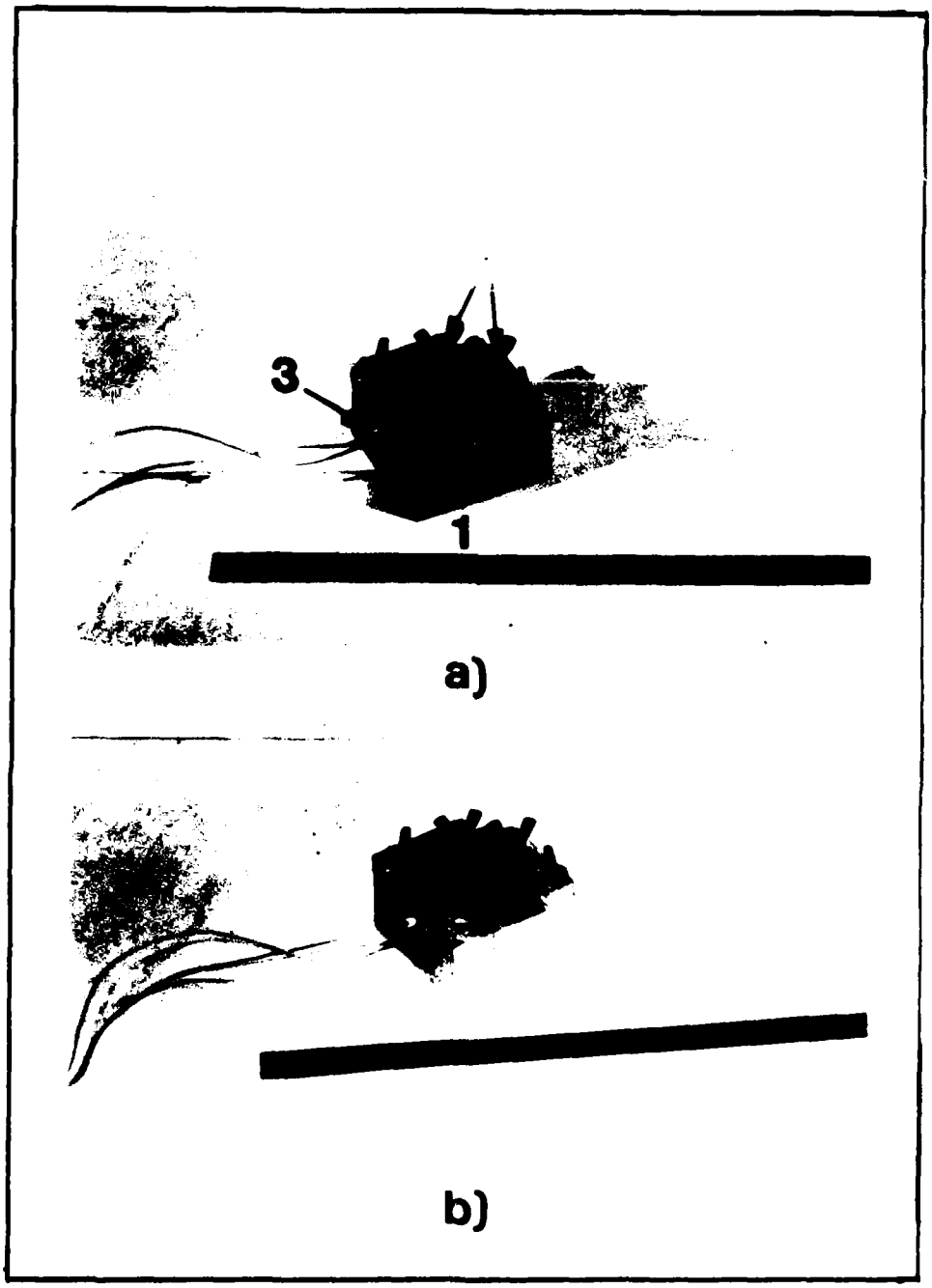


Figure 3-2. Heat Block Used In the Eutectic Bonding Process
a) This photograph shows the block with the:
   1) raised area for localized heating under the wells,
   2) alignment guides, and
   3) the location of the thermocouple.
b) This photograph shows a quartered 3 inch wafer positioned on the raised area.

The wafers were precisely etched to well depths of 9 mils (2[illegible] microns) in the 3 x 3 matrix pattern of square (240 mil by 240 mil) wells

Square pieces (100 mils by 100 mils) of silicon wafer with a 3[illegible] mil thickness (thickness measured with a micrometer (Brown & Sharpe, New York, NY)). These pieces were used as phantom IC die for bonding into the wells.

Procedure for Bonding With the Eutectic Materials. The following section describes the procedure used for bonding the phantom die into the wells using the gold eutectic preforms:

1. Initially all materials were thoroughly cleaned. The wafers, preforms, and die were cleaned using the standard clean process (#1 in Appendix D), thoroughly rinsed in deionized water, and baked in an oven for 3 or more hours at 150 degrees Celsius. Only the materials to be used were removed from the oven; care was taken to avoid contaminating the samples.
2. Samples were prepared by placing a single preform in the bottom of the wells. A die was then placed on top of each preform. Theoretically, 0.5 mils of the die extends above the plane of the top surface of the substrate. The thickness of the die (7.5 mils) plus the thickness of the preform (1.5 mils) is 0.5 mils greater than the 9.0 mil depth of the etched wells.
3. The heat block is placed on the hot plate, the plate turned on, and the heat block temperature verified and manually adjusted to the desired temperature. Three different temperatures were examined; one for each of the three eutectic gold alloys). The

heat block's temperature was calibrated earlier, and the details of this calibration are presented in Appendix F.

4. When the block was at the desired temperature, the sample was placed on the heat block, a glass photomask blank was placed on the sample, and the weight placed on the glass mask. The glass and weight provide a downward force which acts to press the die into the molten eutectic material. The cure times were on the order of 15 seconds. The sample was then removed (after removing the glass and weight) and allowed to cool to room temperature. The solidification of the adhesive should take place quickly.

Each of the three eutectic materials were evaluated; the performance results of this bonding evaluation are presented in Chapter IV.

Application of Ultrasound Vibration to Enhance Bonding. Since no scrubbing action was possible because of the tight fit of the die in the wells, ultrasound vibration was applied to the heat block to discern if the vibrations would enhance the bonding process. This processing feature was readily accommodated in the fabrication procedure. That is, after the heat block was at the desired temperature, it was quickly placed in contact with the ultrasound vibration. No method of assessing the coupling coefficient of the ultrasonic source to the heat block/sample was attempted. The sample was placed on the block before the temperature dropped below the eutectic point.

Epoxy Bonding Equipment and Materials. The following equipment (illustrated in Figure 3-3) was used to evaluate the performance of the epoxy adhesives:

1. Vacuum chuck and vacuum pump. This was used to hold the substrate stable when the die were inserted.
2. Hot plate with a 0-400 degree Celsius range.
3. Tweezers for die handling.
4. Forced air oven with a 0-350 degree Celsius range.
5. Several two inch by two inch glass photomask blank plates and a 100 gram weight.

The following materials were used: 1. The epoxies described in the previous section.

2. Substrates and die identical to those described under the section titled Eutectic Bonding Equipment and Materials.

Procedure For Bonding With Epoxies. The following section describes the procedure used for bonding the die into wells using the epoxies.

1. The wafers and die were cleaned using the standard clean procedure (#1 in Appendix D), thoroughly rinsed in deionized water, and baked for 3 or more hours at 150 degrees Celsius. Only the materials to be used were removed from the oven; care was taken to avoid contaminating the samples.
2. The samples were prepared by placing a single substrate on the vacuum chuck. A matrix (3 x 3) of small dots of epoxy (if single component epoxy, it needs to be thawed prior to use; if a two component epoxy, it needs to be mixed prior to use) are placed on the bottom surface of each well using the tip of a toothpick to

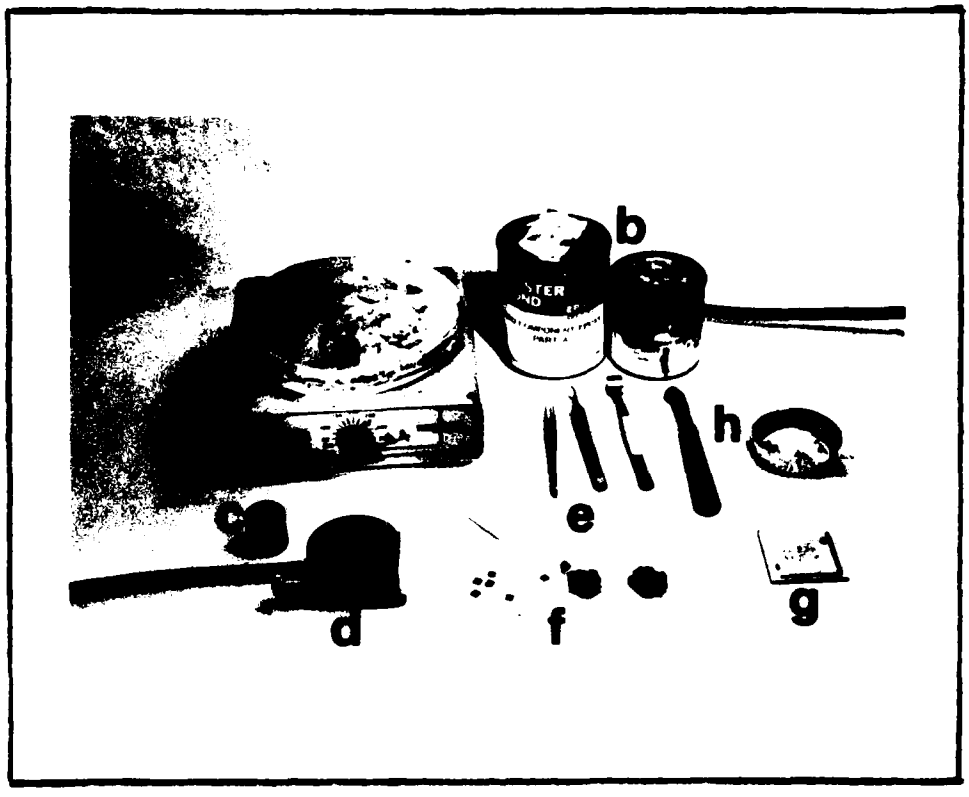


Figure 3-3. Equipment Used in the Epoxy Bonding Process.
a) Hotplate with 0-400 degrees Celsius range,
b) Adhesive (Master Bond EP34CA Special featured in photograph), c) 100 gram weight,
d) Vacuum chuck to hold wafer during preparation,
e) Tweezers, toothpicks for application, f) Die,
g) Glass photomask, and h) Epoxy mixing knife and bowl.

apply the material. It was difficult to dispense the correct (and consistent) amount of epoxy. Therefore, trial and error experimentation was employed to determine the approximate amount of epoxy needed for an effective bond.

3. Each individual die had its backside "painted" with a transparent, thin coat of epoxy to wet its surface. It was then placed into a well with tweezers. The entire substrate was either placed in a forced air oven (125-150 degrees Celsius) or placed directly on a hot plate (125-150 degrees Celsius). The former curing technique was used initially; later, however, the hotplate was used exclusively since the results appeared to be the same, and the sample could be visually monitored while on the hot plate. The curing times were approximately one hour for each of the epoxies tested. While in the oven or on the hotplate, a glass and weight was place on each sample to restrict the movement of the die to the region below the plane formed by the substrate's top surface. After cure, the glass and weight were removed and the substrates were allowed to cool.

Silver Glass Bonding Equipment and Materials. The following equipment was used to evaluate the performance of the silver glass adhesives:

1. Vacuum chuck and pump. This arrangement was used to hold the substrate stable while the adhesive and die were inserted.
2. Thermal oxidation furnace tube set at 435 degrees Celsius.
3. Tweezers for die handling.

The following materials were used:

1. The silver glass adhesive describe in the previous section.

2. Substrates and die identical to those described in the section titled Eutectic Bonding Equipment and Materials.

Procedure for Bonding With Silver Glass. The following section describes the procedure used for bonding the die into wells using the silver glass adhesive:

1. The wafers and die were cleaned using the standard clean procedure (#1 in Appendix D), thoroughly rinsed in deionized water, and baked in a forced air oven for 3 or more hours at 150 degrees Celsius. Only the materials to be used were removed from the oven: care was taken to avoid contaminating the samples.
2. Samples were prepared by placing a single substrate on the vacuum chuck. A matrix (3 x 3) of small dots of the adhesive material was placed on the bottom surface of each well using the tip of a toothpick to apply the material. As with the application of epoxy, it was difficult to determine the correct amount of material to be deposited. Again, trial and error experimentation was completed to determine the optimum amount.
3. Each individual die was placed into its well with tweezers, and the entire substrate was placed on a quartz platform to facilitate insertion into the oxidation tube. The glass photomask and weight were then placed on the sample to provide alignment of the die and the substrate.
4. A temperature profile of the oxidation tube was measured before the sample was processed. The results of this calibration are presented in Figure 4-15 in Chapter IV. The platform was slowly inserted into the tube according the schedule given below:

a. Place the sample on the port of the furnace tube for 6 minutes. The port of the tube is defined for this procedure to extend 1.5 inches from the tube's outer edge.

b. Slide the sample into the tube to a point 5 inches from the outer edge at the rate of about one inch every 90 seconds. Remain at this position for 30 seconds.

c. Insert the sample further into the tube to a point 12 inches from the outer edge of the tube at a rate of 1 inch per minute. Remain at this position for 6 minutes.

d. Slowly remove the sample from the tube, using an extraction rate of 1 inch per minute.

This schedule was derived from the manufacturer's literature. After this thermal cure cycle, the substrates were removed and allowed to cool.

Sample Evaluation of the Die Attach Adhesive Study. The following methods were used to evaluate the samples fabricated in the Die Attach Adhesive Study.

Pry test. A simple pry test was administered to the cured samples to eliminate an adhesive candidate not strong enough to resist a mild prying action. A calibrated force meter (No model number, Jonard Industries Corp., Bronx, NY) (illustrated in Figure 3-4) with a thin knife-like tip was inserted between the edge of the die and the sidewall of the well, and a prying action was applied. If the die separated from the well, the amount of force was recorded from the meter. If the meter attained its maximum reading of 150 grams of force, the test was terminated and the adhesive candidate was considered to have passed.

Cross-Sectional Scanning Electron Microscope Evaluation of the Adhesives. The adhesives passing the pry test were evaluated for voiding

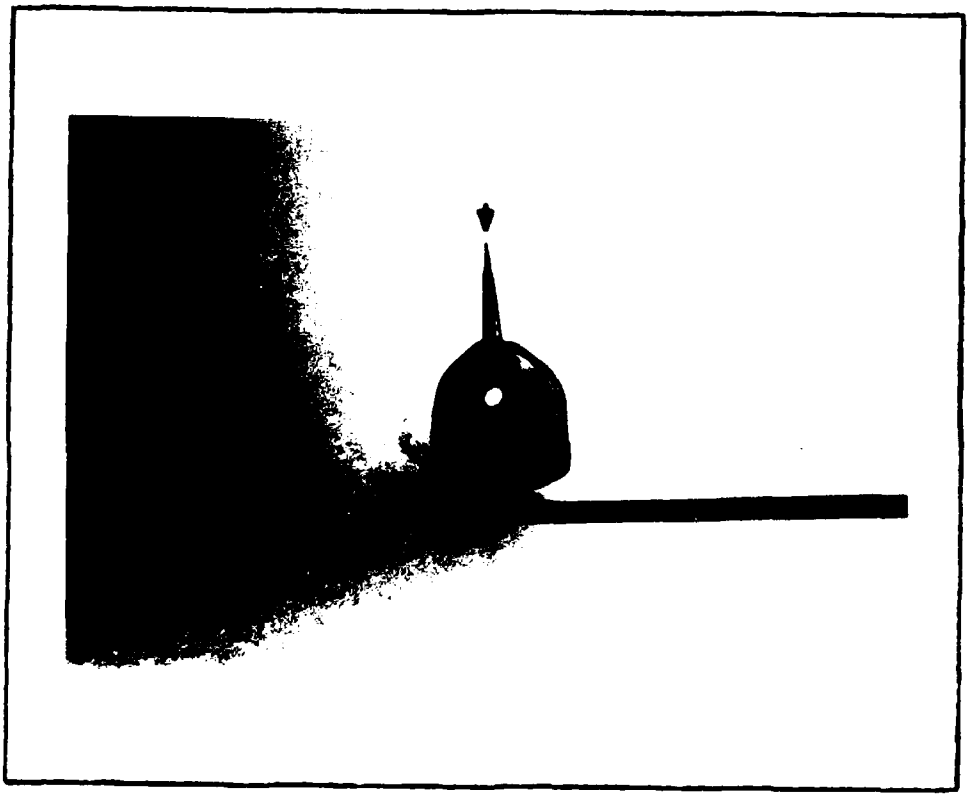


Figure 3-4. Force Meter (0-150 grams) Used in the Pry Test. Arrow points to tip inserted between bonded die and support wafer. Force of prying action is read from the dial.

by examining the cross-sections of the cured adhesive under a scanning electron microscope (SEM) (ISI WB-6, International Scientific Instruments, Inc., Milpitas, CA). Twenty mil thick strips of the samples were cut with a dicing saw (Model 602M, GS Microautomation, Inc., Fremont, CA). The strips containing areas for observing the die-to-substrate bond were mounted onto SEM specimen tabs. SEM micrographs characteristic of the adhesive void frequency were taken and presented in Chapter IV.

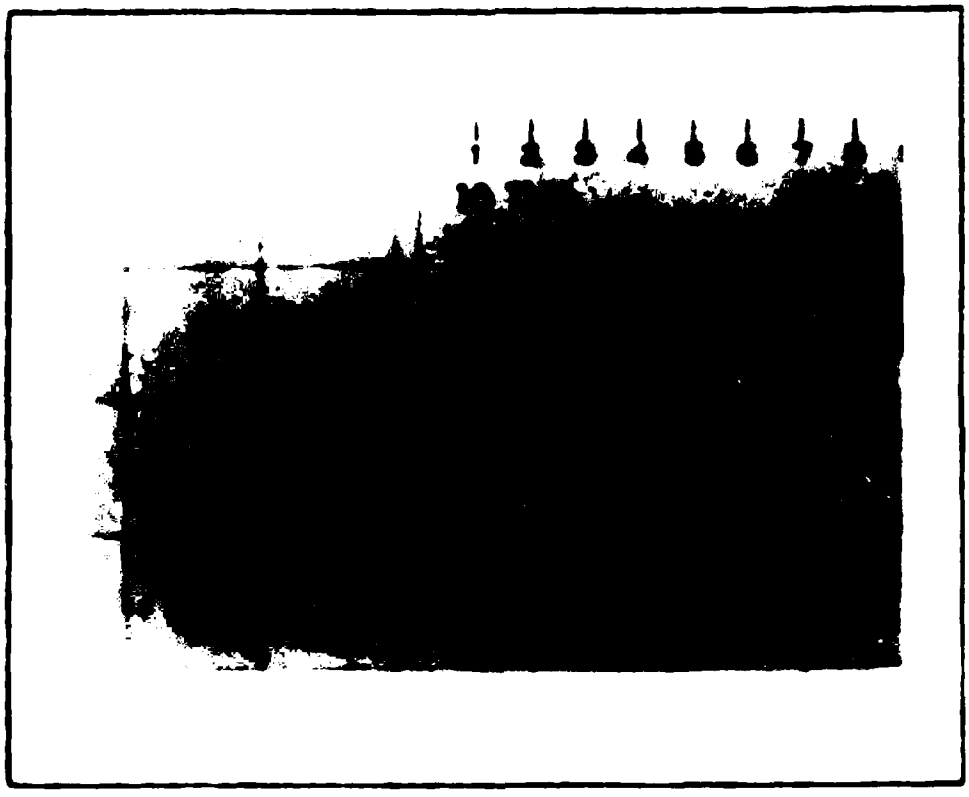
Fabrication Of Samples For Electrical Testing.

With the Wet Orientation Dependent Etching (WODE) and Die Attach Adhesive (DAA) studies complete, the focus turned to the fabrication of working samples for electrical testing and fault analysis. The results of the WODE study were incorporated into the procedure for fabricating the final samples. All etching subsequent to this point in the research was accomplished using the combination of quartered 3-inch (100) wafers and the buffered potassium hydroxide etchant. Further, as a result of the positive features of the two-component epoxy (Master Bond EP-1-A) observed in the DAA study, it was used exclusively as the die attach adhesive in subsequent experimentation.

The fabrication of working samples involved conducting several trial experiments; each provided information on the proper procedures needed to define and mature the Hybrid Wafer Scale Integration (HWSI) process. The following section provides a description of these experiments to include the equipment, materials, and procedures used.

Die Preparation. For all further experiments, a supply of 100 die (with patterned circuits) were prepared. The silicon wafers [illegible]

68ID981, Monsanto, Inc., Palo Alto, CA, used to prepare the die [illegible] orientation were n-type phosphorus doped [illegible] ohms square resistivity, and [illegible] inches in diameter. [illegible]



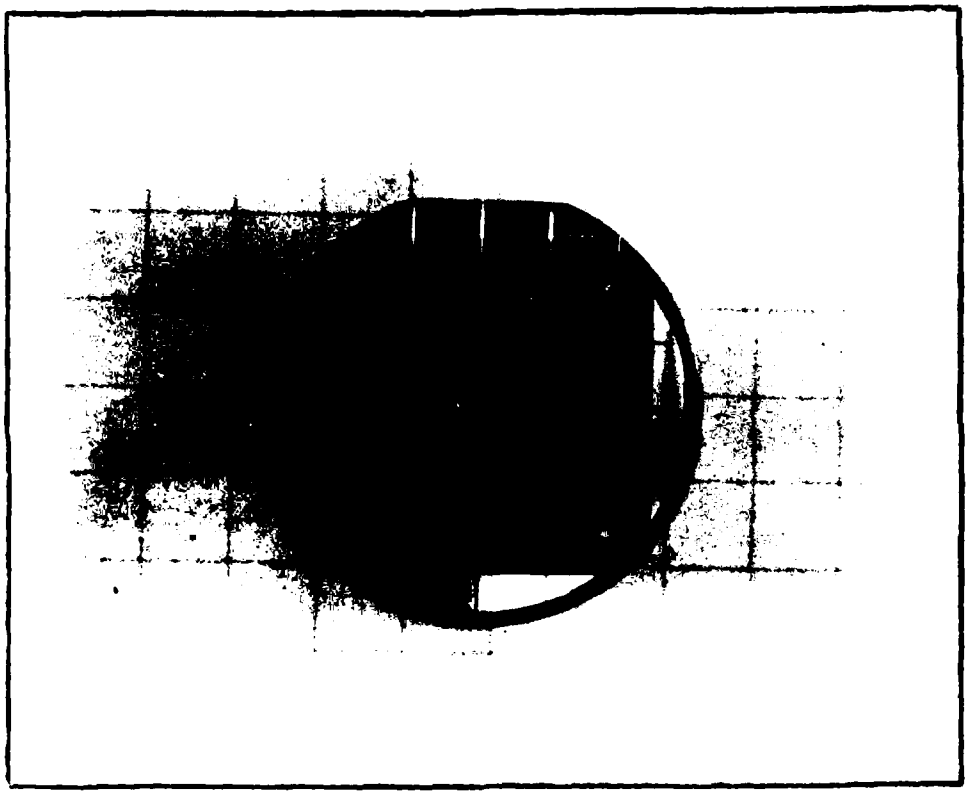


Figure 3-6. A Wafer of Cut but Undiced Die. Sixteen die were prepared on each wafer. The magnification factor is 1.875X.

Calculation of Well Dimensions. Before using the anisotropic etching methodology realized from the WODE study, it was necessary to specify the well's depth and the well's mask dimensions. An ideally fabricated well will be as deep as the average thickness of the die used, plus a prescribed thickness to accommodate the cured die bond adhesive. The die fabricated in the previous step were selected to be 8.7 mils thick. Assuming the prescribed thickness of the EP-34CA Special epoxy to be 1.0 $\pm$ 0.2 mils, the desired well depth is 9.7 mils.

Since the die are 197 mils by 197 mils, the well's surface dimensions need to be at least this size to assure proper mounting of the die. The openings in the oxide mask will determine the dimensions of the upper opening of the well (W_o in Figure 3-7). If the desired size of the well's surface opening is 200 mils by 200 mils square, the following equations can be used to calculate the dimensions of the oxide mask, and consequently, the size of the photolithography mask features. To determine W_o, Figure 3-7 reveals that:

$$W_o = [(-2 \sin \theta)(R_{111})(t)] + W_t \qquad (3\text{-}1)$$

and

$$W_t = W_b + (2 / [(\tan \theta)(R_{100})(t)]) . \qquad (3\text{-}2)$$

Therefore:

$$W_o = W_b + (2 / [(\tan \theta)(R_{100})(t) - (\sin \theta)(R_{111})(t)]) \qquad (3\text{-}3)$$

where W_o is the width of the oxide opening along one edge, W_t is the width of the well's opening beneath the oxide mask, W_b is the critical size of the well along one edge, θ is the angle formed between the plane of the well's surface and the sidewalls, R_{111} is the rate that the silicon etches in the <111> direction, R_{100} is the rate that the silicon

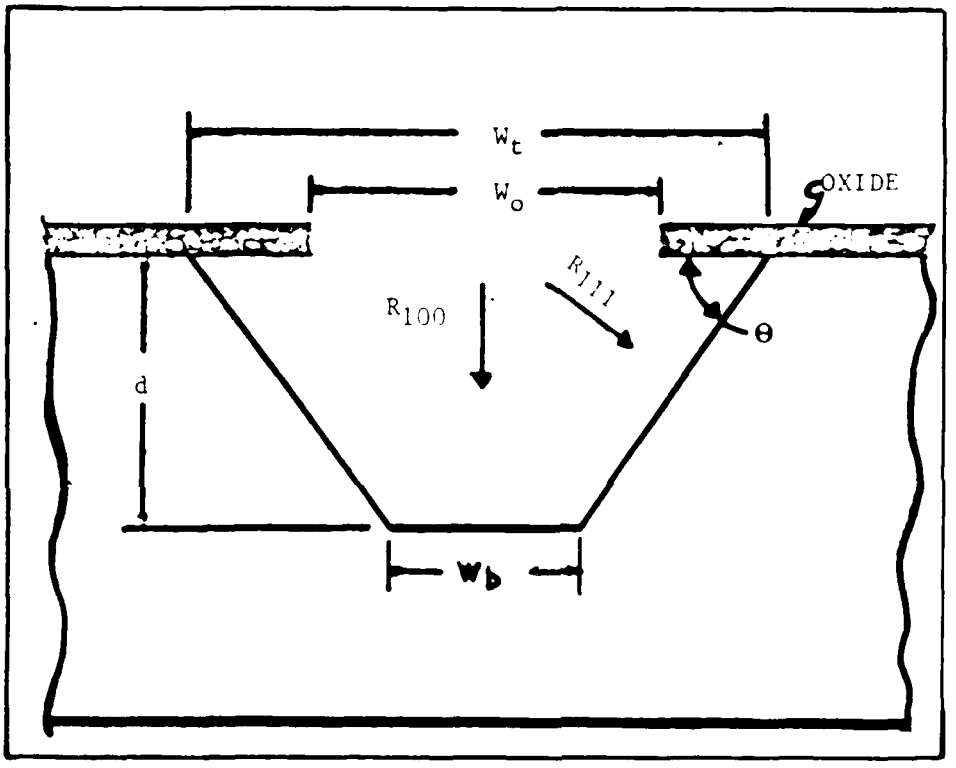


Figure 3-[illegible] cross-sectional illustration of a [illegible]

Wo is the width of the mask opening

Wt is the width of the well opening at the surface

Wb is the width of the well bottom

d is the depth of the well

θ is the angle of the sidewall to the wafer plane

R100 is the etch rate in the <100> direction

R111 is the etch rate in the <111> direction

etchs in the <100> directions, and t is the time that the wafer is immersed in the etchant (18:3-1, 349).

Many of the variables in Equations (3-1, 3-2, and 3-3) were determined in the WPAFB study. The angle θ was found to be approximately 54.7 degrees, which is slightly less than the 54.74 degrees predicted theoretically. The rate of etching in the <100> directions (normal to the surface of the <100> wafers) was determined to be approximately [illegible] microns per minute. The rate R_{111} of etching in the <111> direction was not investigated in the WPAFB study. Price has reported the etch rate to be [illegible] Angstroms per minute (18:3-1). The time that the wafers are [illegible] is important in the control of the depth of the wells and the [illegible] rate R_{111}. As [illegible] the [illegible] well depth [illegible] microns. If the [illegible] rate is [illegible] the time required to complete the etch is [illegible] minutes.

__Etching of Wafers for Final Samples__. With the well dimensions specified, the required masks were fabricated. Six 3-inch (100) silicon wafers (lot #18143A/6977, p-doped, 30-60 ohm per square sheet resistance, [illegible] mil thickness, Aurel, Inc., Santa Clara, CA) were quartered using a [illegible] dicing saw. Extreme care was taken to assure that the cuts were made along the (100) planes. This requirement was accomplished by carefully aligning the cuts parallel to the wafer's primary flat. The quartered wafers were then cleaned (standard clean #1, Appendix D) and oxidized (see Appendix C) with an oxide thickness of 1.5 microns. Using standard photolithography processes (Appendix C), the oxide masks were fabricated. Again the wafers were cleaned (standard clean #1, in Appendix D) and stored in deionized water until etched.

Etching of the wafers was conducted using the procedure presented in the W[illegible]F study.

1. The etchant used was a buffered potassium hydroxide solution prepared using the following concentrations and procedures:

   a. [illegible] % (by weight) potassium hydroxide,

   b. [illegible] % (by weight) deionized water,

   c. [illegible] % (by weight) isopropyl alcohol, and the result was [illegible] degrees [illegible] degrees Celsius.

2. The [illegible] wafers were placed in the etchant and [illegible] [illegible] time of [illegible] and 33 minutes.

[illegible]

[illegible] the wafers were [illegible]

[illegible] water.

5. The wafers were inspected for etching defects. The well depths were measured and compared to the desired results. If further exposure to the etchant was needed, it was accomplished.
6. All wafers were then stripped of their oxide masks (20 minutes in buffered hydrofluoric acid) and re-oxidized (see Appendix C) to an oxide thickness of 0.12 microns. This step was accomplished to provide a compatible surface for the die bond adhesive and polyimide layer to adhere to.
7. Once the etching and oxidation processes were completed, the wafers were divided into groups according to their quality (quality wafers for the preparation of final samples, slightly defective wafers used for processing experiments, and defective wafers were discarded) and stored in closed containers.

Evaluation of the Results. Six of the quality wafers were chosen at random, and the size of the well's surface dimensions were measured. The well's surface dimensions were measured using the Coordinatograph which has the capability of measuring dimensions to 1 mil accuracy. To accomplish this measurement, the alignment scope was inserted, and the wafer was placed on the glass table with its flat parallel to the Coordinatograph's x-axis. While moving the scope along the x-axis, the edge being measured was kept in view on the alignment scope by manually adjusting the wafer's position on the glass table. The scope was then moved to one corner of a well and centered precisely on the well's corner (at the well's surface). Both values on the digital meter were reset. The scope was then moved along the well's edge in the x-direction until it met the adjacent corner. The scope was again precisely aligned with respect to the center's corner. The x-dimension

length was then recorded from the digital meter. This procedure was then repeated for the dimension in the y-direction. This procedure was repeated for all six wells on each of the six wafers. The measurements are presented in Chapter IV.

Die Attach Procedure. With a supply of wafers prepared for further processing, attention was focused toward preparing a number of final samples by bonding die into the six wells. A description of the procedure follows. Information concerning equipment and materials not previously introduced is included.

Calculation of Epoxy Volume. Based on the results of the previous section, it is known that the typical well has a flat surface approximately 202 ± 2 mils square and a depth of 244 ± 1 microns (9.64 ± 0.03 mils). The die were determined to be 8.7 ± 0.3 mils thick and 197 mils by 197 mils square. Assuming that the die's top surface is co-planar with the top surface of the support wafer, the minimum volume of space needed to be filled with epoxy (when 9.0 mil thick die are placed in a 9.61 mil deep well) was calculated to be 2.44×10^{-6} square inches or 0.400 microliters. The maximum volume (when 8.4 mil thick die are placed in wells which are 9.67 mils deep) was calculated to be 50.8×10^{-6} square inches or 0.832 microliters. Assuming a mean value for both the die thickness (8.7 mils) and well depth (9.64 mils), the average volume is 38.4×10^{-6} square inches or 0.630 microliters. Assuming epoxy shrinkage to be approximately 30% (22:307), the required epoxy volumes are:

Minimum	0.570	microliters
Average	0.900	microliters
Maximum	1.190	microliters.

These calculations are, of course, estimates. The volume of epoxy needed can be generally estimated to be about 1 $\pm$ 0.4 microliters. Epoxy dispensing equipment capable of this accuracy was not available. Therefore, the application of the proper amount of die bonding adhesive was more an art than a science. The procedure for mounting the die was the same as that used in the DAA study for applying the EP-34CA Special adhesive. Trial and error experimentation led to a subjective judgement of the proper amount of epoxy to apply in each well. The procedure used for bonding the die into the wells using the epoxy was as follows:

1. The wafers and die were cleaned using the standard clean procedure (#1 in Appendix D), thoroughly rinsed in deionized water, and baked for 3 or more hours at 150 degrees Celsius. Only the materials to be used were removed from the oven; care was taken to avoid contaminating the samples.
2. The samples were prepared by placing a single substrate on the vacuum chuck. A matrix (3 x 3) of small dots of epoxy (the two-component epoxy needs to be mixed prior to use) were placed on the bottom surface of each well using the tip of a toothpick.
3. Each individual die had its backside "painted" with a transparent, thin coat of epoxy to wet its surface. It was then placed into a well with tweezers. The entire substrate was transferred directly to the hot plate (125-150 degrees Celsius) for a two minute cure. The heat cycle fluidized the epoxy. The glass cover and weight were placed on the sample to press the die into the epoxy and to restrict the movement of the die to the region below the plane formed by the substrate's top surface. The excess epoxy repositioned itself in the gap region. The glass and

weight were then removed, and the sample was removed from the heat source. While cooling on a nearby table, the glass and weight were again placed on the sample.

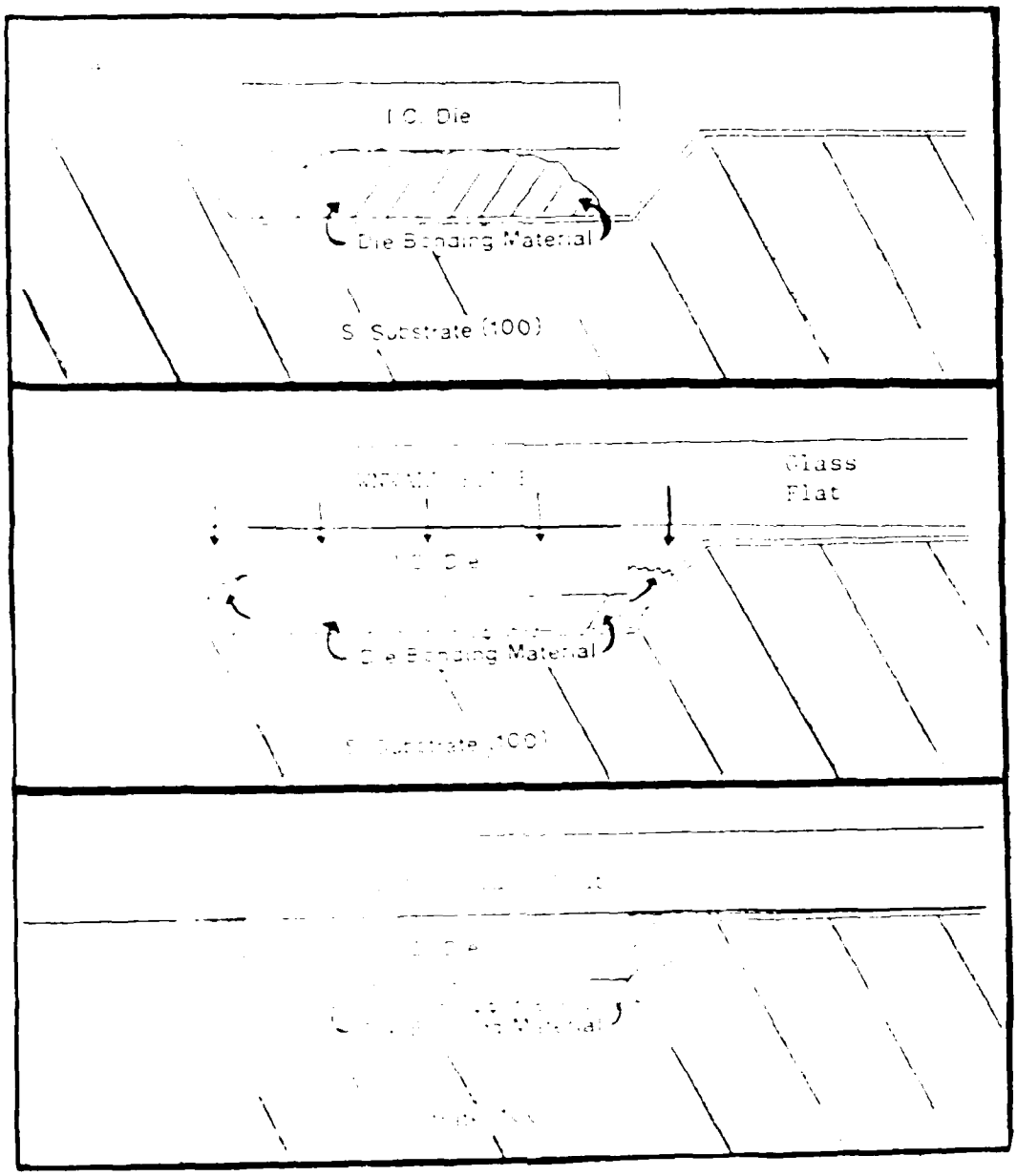
4. If too much epoxy was dispensed into the well, it flowed out of the gap and onto the cover glass surface. This excess epoxy (now cool) was removed with acetone and a cotton swab. The glass was also cleaned with acetone and a swab. Steps 3 and 4 were repeated until no excess epoxy was found on the glass. This procedure was often implemented 3-4 times.
5. The sample was allowed to cure on the hotplate for 30 minutes with the glass and weight in place, and then 30 additional minutes without the glass and weight. After cure, the sample was removed and allowed to cool.

This process is illustrated in Figure 3-8. Each die was positioned onto the thick epoxy (a) dispensed into the well (as described in step 3 above), and as the weighted glass optical flat (2 inch square photomask) was placed on the die, the downward force caused excess epoxy to move into the gap region. Since the epoxy becomes more fluidic with heat, the redistribution of excess epoxy occurred very quickly (b). During the final cure (c), the flat remained in position preventing the die from rising out of position due to pressures generated from trapped solvent vapors. After approximately 30 minutes, the flat was removed, and the sample was allowed to cure without the aid of the flat. The post-cure samples were expected to have a meniscus at the gap's surface.

Evaluation of Master Bond EP-34CA Special as Gap Filler. The cost of Master Bond EP-34CA Special was also evaluated as the gap filler

illustrated in Figure 3-8, any excess epoxy can [illegible] into the gap surrounding the die. Typically, enough [illegible] displaced from under the die so that the gap volume is filled [illegible] after cure (all shrinkage has taken place), a meniscus [illegible] a need for more epoxy to completely fill the gap. The [illegible] applying additional epoxy to the gap was implemented [illegible]

1. The wafer was mounted on the vacuum chuck [illegible] epoxy (a drop approximately a quarter [illegible] placed in the center of the 3x3 matrix [illegible]
2. The wafer was transferred to the hot plate [illegible] degrees Celsius. As the epoxy was heated [illegible] Using an clean toothpick, the liquid epoxy was [illegible] over the gap areas on the wafer. As it [illegible] cover the gap areas, it was transferred [illegible] result, epoxy [illegible]
3. The wafer was [illegible] room temperature. [illegible]



with glass in place.

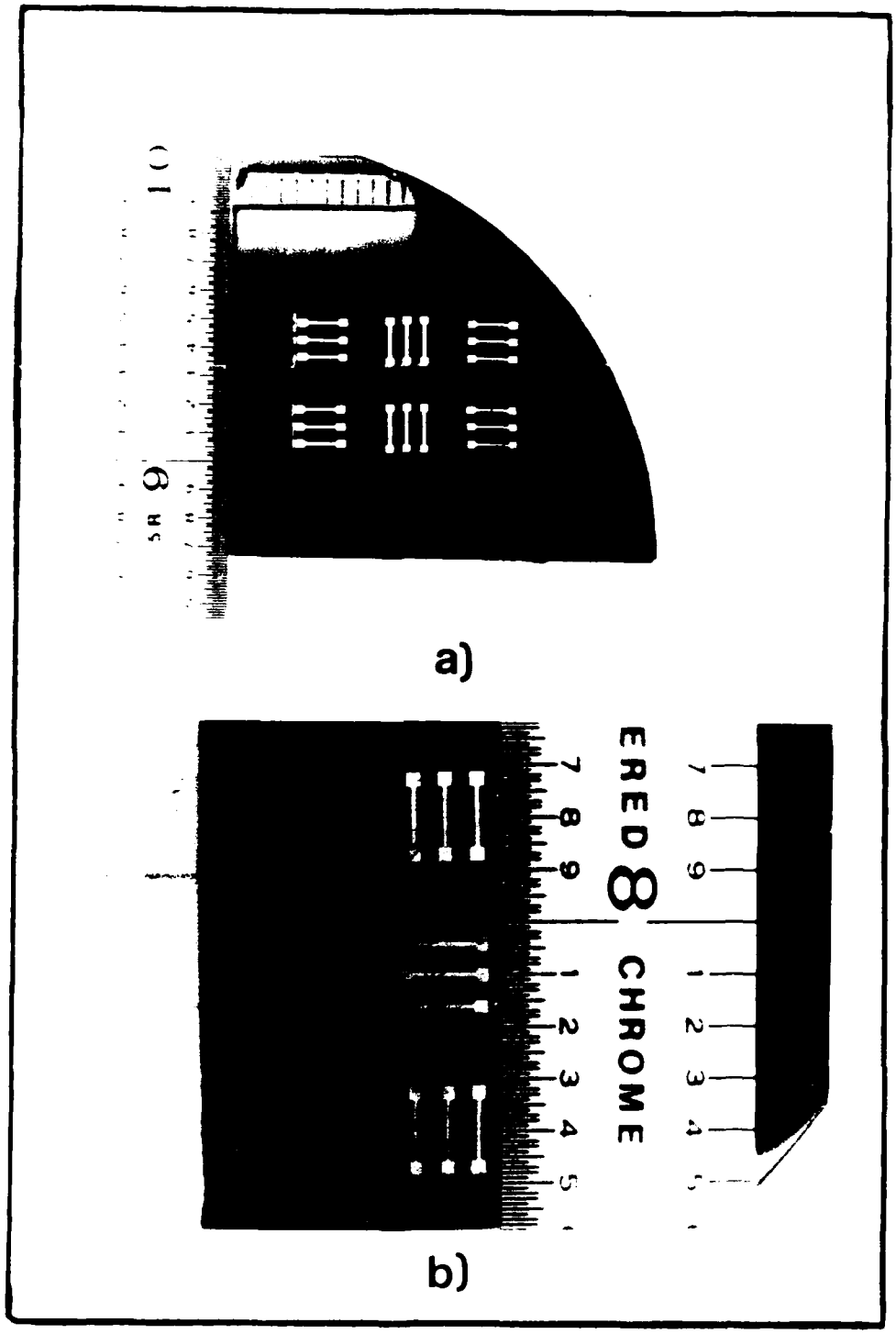


Figure 3-9. A Typical Sample Before Application of Polyimide. a) Full view, the magnification factor is 1.6X; and b) Close-up view, the magnification factor is 3.0X.

Effect of [illegible] temperature [illegible] Master Board [illegible] degrees ± 5 degrees Celsius. To determine the effects of higher processing temperatures on the epoxy [illegible] experiment was conducted.

1. Two wafers (all six die bonded and the gap surrounding the die filled) were tested. Initially, the difference or delta between the surface of the support wafer to the surface of the die was measured at 12 sites. Figure 3-10 illustrates the concept of the delta measurement and the locations of the 12 measurements. The measurement was accomplished with the optical microscope. By focussing on the two planes and comparing the readings observed on the calibration knob, the difference was determined with an accuracy of ± 3 microns.
2. Sample A was heated in a forced air oven at 350 degrees Celsius for 1 hour with a 2 inch square optical flat (photomask) and 50 gram weight positioned to keep the die in place. The sample was allowed to cool, and the delta measurements were taken. This experiment was accomplished to determine the initial effect of high temperature.

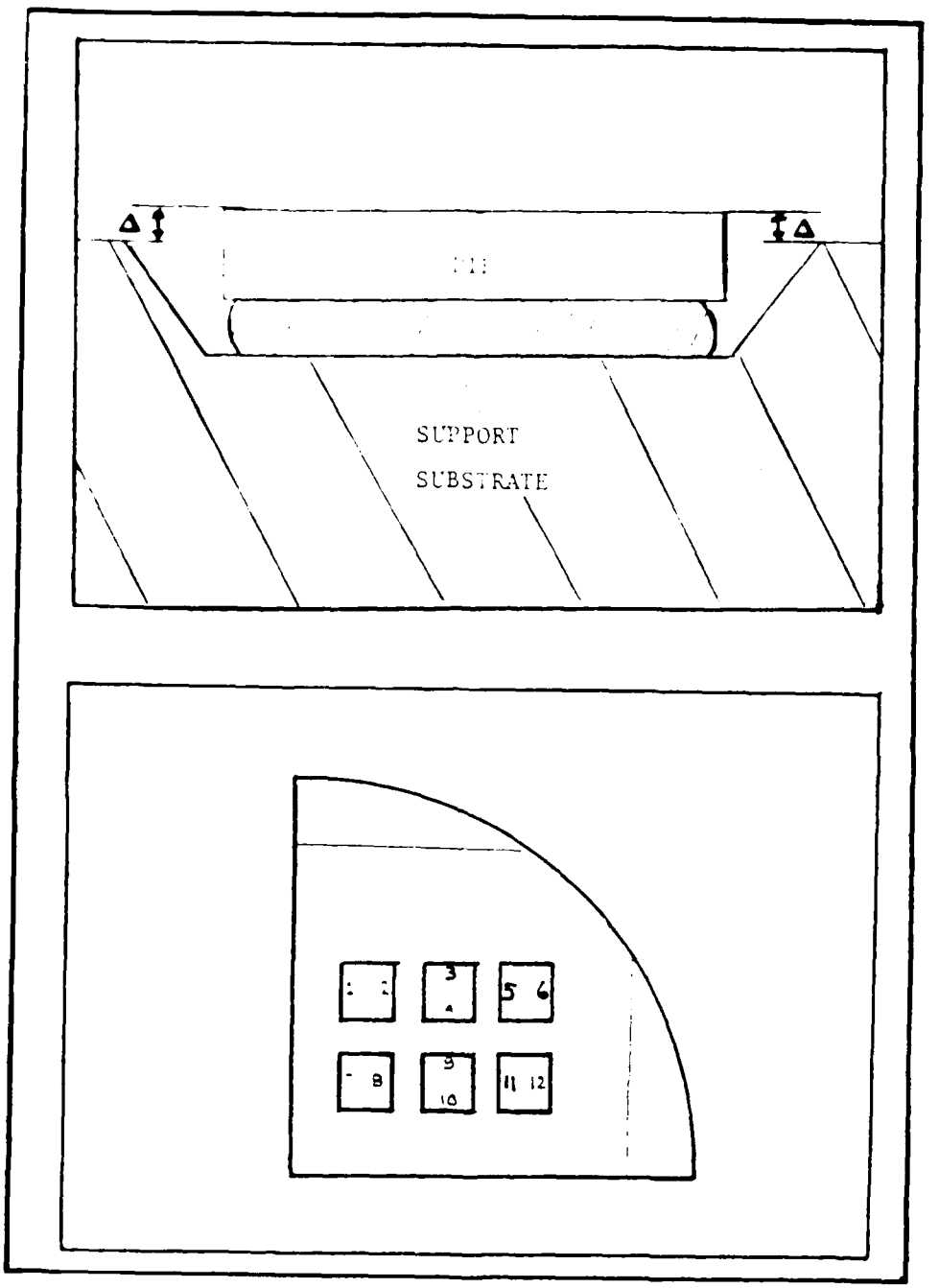


Figure 3-10. The Delta Measurement Scheme.
a) The delta (Δ) separation is the vertical difference in microns between the plates of the support substrate and the die, and b) the twelve sites where the delta measurements were made on each sample

3. Sample A was again heated to 350 degrees Celsius for 1 hour without the glass and weight. The sample was allowed to cool and the delta measurements were taken. This experiment was accomplished to determine the effect of reheating without the constraint of the cover glass and weight.

4. Sample B was heated in the forced air oven in 25 degree Celsius increments, starting at 150 degrees Celsius and ending at 350 degrees Celsius. The samples remained at each temperature for 30 minutes. This experiment was accomplished to determine, within 25 degrees Celsius the highest permissible processing temperature.

The results of these experiments are presented in Chapter IV.

Application of Photosensitive Polyimide as a Planarizing Film and Inter-Metal Insulator. The photosensitive polyimide (HTR 3-200) was used for an inter-metal insulator because of its excellent ability to planarize rough or irregular surfaces. The HTR 3-200 polyimide is also capable of being applied in a relatively thick layer (2-80 microns). In addition, the polyimide is photosensitive, so vias can be realized using a minimum number of processing steps. The process used to apply the HTR 3-200 polyimide to the top surface of the final samples is described in Appendix I.

Via Fabrication Experiment. The Merck HTR 3-200 vendor's literature indicates that proximity photolithography is superior to contact photolithography for achieving sloping vias. To determine the optimal proximity distance for producing vias in the final samples, and the effect of annealing them and the metallic interconnections, the following experiment was conducted

1. Four 2-inch wafers ((111) orientation, n-doped, Monsanto, Inc., St. Louis, MO) were cleaned using the standard clean process (#1 in Appendix D) and oxidized to a thickness of 2000 Angstroms, (Appendix C).

2. Aluminum was evaporated on oxidized samples [8000 Angstroms thick as measured with the Dektak profile meter (Model 900051, Sloan Technology Corporation, Santa Barbara, CA)] using the techniques detailed in Appendix G.

3. Merck Selectilux HTR 3-200 photosensitive polyimide was spun on the wafers at 1000 rpm for 30 seconds and prebaked on a hot plate at 100 degrees Celsius for 20 minutes. The preimidization thickness of the layer was approximately 40 microns. The wafers were now ready for photolithography. (Further details on the application of the photosensitive polyimide are given in Appendix I).

4. The via mask (Appendix B, Figure B-3) was used for the photolithography processes. On one of the four wafers (sample A), the via pattern was exposed using contact printing. On samples B, C, and D, proximity exposure was used. The spacing between the polyimide layer and the mask was achieved by using layers of mylar film (each film has a 4.5 mil thickness). A notch was cut out of each mylar film layer to allow an air gap during exposure. Sample B was exposed using 3 mylar film thicknesses (13.5 mils total gap); sample C was exposed using 6 film thicknesses (27.0 mils); and sample D was exposed using 9 film thicknesses (40.5 mils). Each sample was then developed according to the vendor's recommended procedure with two exceptions. The samples were

developed on the photoresist spinner using a 2-to-1 spray. A slightly longer development times were provided for sample D to assure complete development of the vias. The vias were inspected visually to determine whether they had completely etched to the aluminum layer beneath the polyimide. Once the vias were "clean", or completely etched through, the aluminum layer was visible.

5. The samples were then cured at 250 degrees Celsius for 1 hour.
6. Next, aluminum was evaporated on the samples (10,000 Angstroms thick as measured with the Dektak profile meter) using the techniques detailed in Appendix G.
7. The metal was patterned using the conventional photolithography and etch technique. The second-level metal mask (Figure B-4 in Appendix B) was used to pattern the aluminum film. The mask was aligned to the vias so that each conductor terminated at a via. Positive photoresist (Shipley M1350J) was spun on the samples at 3000 rpm and soft baked. The samples were then exposed (45 second exposure time), developed, and hardbaked at 150 degrees Celsius for 1 hour. (Appendix C details the photolithography procedure).
8. A continuity test was performed on each conductor on all four samples. On each sample, one of the two probes of the digital ohmmeter (Model 3010UL, Beckman, Inc., Fullerton, CA) was positioned to contact the ground plane (the first aluminum layer evaporated in step 2), and the other probe was contacted with each of the conductor pads. The number of successful

interconnections through the vias and the resistance reading on the ohmmeter was recorded. The results are presented in Chapter IV.

9. The samples were then annealed at 250 degrees Celsius for 1 hour. The continuity tests described in step 8 were again performed on the samples, and the results are presented in Chapter IV.

Application of the Polyimide. Three final samples were coated with the HTR 3-200 polyimide and vias were fabricated in the layer. The polyimide was spun on at 1000 rpm for 30 seconds and allowed to sit horizontally for 10 minutes. The samples were then prebaked in a forced air oven at 65 degrees Celsius for 4 hours. The hot plate method of prebaking the samples was attempted, but it was found to give undesirable results. Small bubbles were generated from the underlying epoxy used to fill the gap when the wafer was heated from the backside. Therefore, the prebake and cure cycles were done only in the forced air oven.

Proximity exposure was used for the fabrication of vias. An air gap of 27 mils was used; this gap was achieved by stacking 6 mylar films. The vias were developed on the spinner at 200 rpm using the Selectiplast HTR D-2 developer (EM Industries, Inc., Hawthorne, NY) (spray with the developer for 40 seconds, rinse with 2-propanol for 10 seconds, and blow dry).

The samples were cured at 250 degrees Celsius in a forced air oven for 3 hours. According to the Merck HTR 3-200 literature, the final polyimide thickness was approximately 20 mils. After cure, the samples were ready for metallization.

Metallization of Samples. Following the application of the polyimide, the samples were coated with a thin layer of aluminum which was then patterned using standard photolithography and etch techniques. The patterning of the interconnects prepared the final samples for electrical testing. The method for depositing the aluminum metal on the surface of the wafers was thermal evaporation. Details of this process are discussed in Appendix G. The photolithography steps can use either positive or negative photoresists. The next section discusses the details concerning the two experiments which sought to determine the optimal aluminum etchant, the type of photoresist to use (positive or negative), and whether annealing should be performed after metal deposition.

Photoresist and Aluminum Anneal Experiment. An experiment was conducted to determine whether positive or negative photoresist provides better results. The effect of annealing the metal prior to patterning and etching was also investigated. The procedure used in this experiment was as follows:

1. Four 2-inch wafers ((111) orientation, n-doped, Monsanto, Inc., St. Louis, MO) were cleaned using the standard clean process (#1 in Appendix D) and oxidized to a thickness of approximately 2000 Angstroms (Appendix C). Merck Selectilux Photosensitive polyimide was spun on the wafers and cured, realizing a cured thickness of approximately 10 mils (Appendix I).
2. Aluminum metal was evaporated on the samples (7500 Angstroms thick) using the techniques detailed in Appendix G.
3. The sheet resistance was measured on all four wafers (designated A, B, C, and D) using an automated resistivity probe (Model AP-150, Veeco Instruments, Inc., Plainview, NY).

4. Samples designated A and C were annealed at 350 degrees Celsius for one hour in a convection oven. Once again the sheet resistance measurements were made.
5. All four wafers were then coated with photoresist. Samples A and B were coated with Shipley MI350J positive photoresist. Samples C and D were coated with Waycoat 28 cps negative photoresist. Each type of photoresist was applied using the vendor's recommended application procedure to achieve a thickness of 2000 Angstroms. The appropriate mask pattern (both positive and negative masks were utilized) used to expose the wafers was the second-level metal mask used throughout the project (illustrated in Appendix B).
6. The samples were then etched to determine which photoresist yielded optimum results. The #2 aluminum etchant heated to 45 degrees Celsius was used (Appendix D). The samples were etched until all exposed aluminum had been removed, and then, they were rinsed in deionized water for 15 minutes.
7. The photoresist was then removed from the aluminum with the Losilux (EM Industries, Inc., Hawthorne, NY) photoresist remover.
8. The final results of the etching process were inspected with an optical microscope. Also, a continuity test was performed on the metal stripes to evaluate their conductivity.

The results of this effort are presented in Chapter IV.

Metallization of the Final Samples. Using the results of the photoresist and aluminum anneal experiment described in the prior section (results reported in Chapter IV), the final samples were metallized and

etched to delineate the metal interconnects for each test circuit. The samples were metallized using the thermal evaporation technique; this procedure is described in Appendix G.

Following the evaporation of aluminum, the samples were annealed at 250 degrees Celsius for 30 minutes. The samples were now ready for patterning the continuous thin film of aluminum into the individual conductors. To achieve this step, the aluminum conducting paths were protected from the aluminum etchant with positive photoresist. The photoresist was spun onto the surface of the aluminum, prebaked, and exposed to ultraviolet light with a photomask shielding those areas to be stripped of metal. A difficulty arises if the photoresist fails to adequately protect the metal where the metal passes over the transition region between the support substrate and the mounted die. The etchant tends to remove the metal from these unprotected areas and produce open circuits. Single and multiple photoresist layers were explored to achieve the desired results.

Single Photoresist Layer. A single layer of Shipley M1350J positive photoresist was spun on one sample. The spinner speed was 2000 rpm to achieve a thick layer of photoresist. The photoresist was prebaked, exposed, and developed. The photoresist left to protect the conductors was post-baked at 180 degrees Celsius for 90 minutes. The photoresist layer was inspected under an optical microscope for areas where the thickness of the resist was inadequate to protect the metal. Particular attention was given to the transition areas between the support substrate and the die.

Multiple Photoresist Layers. A second layer of photoresist was deposited over the first layer and patterned. After postbake, the photoresist was again inspected under an optical microscope for thin areas. This procedure was again repeated for a third time. The results of the three inspections are presented in Chapter IV.

Patterning of the Final Samples. The final samples A, B, and C were patterned using the techniques described above. The metal conductors were protected by a triple layer of photoresist before etching.

Etching of the Aluminum. After the final samples were coated with a triple coat of positive photoresist and postbaked, they were etched in a fine-resolution aluminum etchant (Appendix D). The results of this etching process are presented in Chapter IV.

Removal of the Photoresist. After patterning, the photoresist was removed with Losolin (EM Industries, Inc., Hawthorne, NY) photoresist remover.

Evaluation of the Final Samples.

Three samples (referenced as A, B, and C) were prepared successfully using the procedures described in the previous section. In order to determine the effectiveness of the process, these samples were subjected to various electrical and thermal tests. These tests are described in the next section.

Numbering the Circuits. In order to reference a particular circuit or die on a sample, the circuits were numbered according to the guide presented in Figure 3-11. Circuits 1, 2, and 3 are on die #1; circuits 4, 5, and 6 are on die #2; and so on. Die #1 is the die in the center

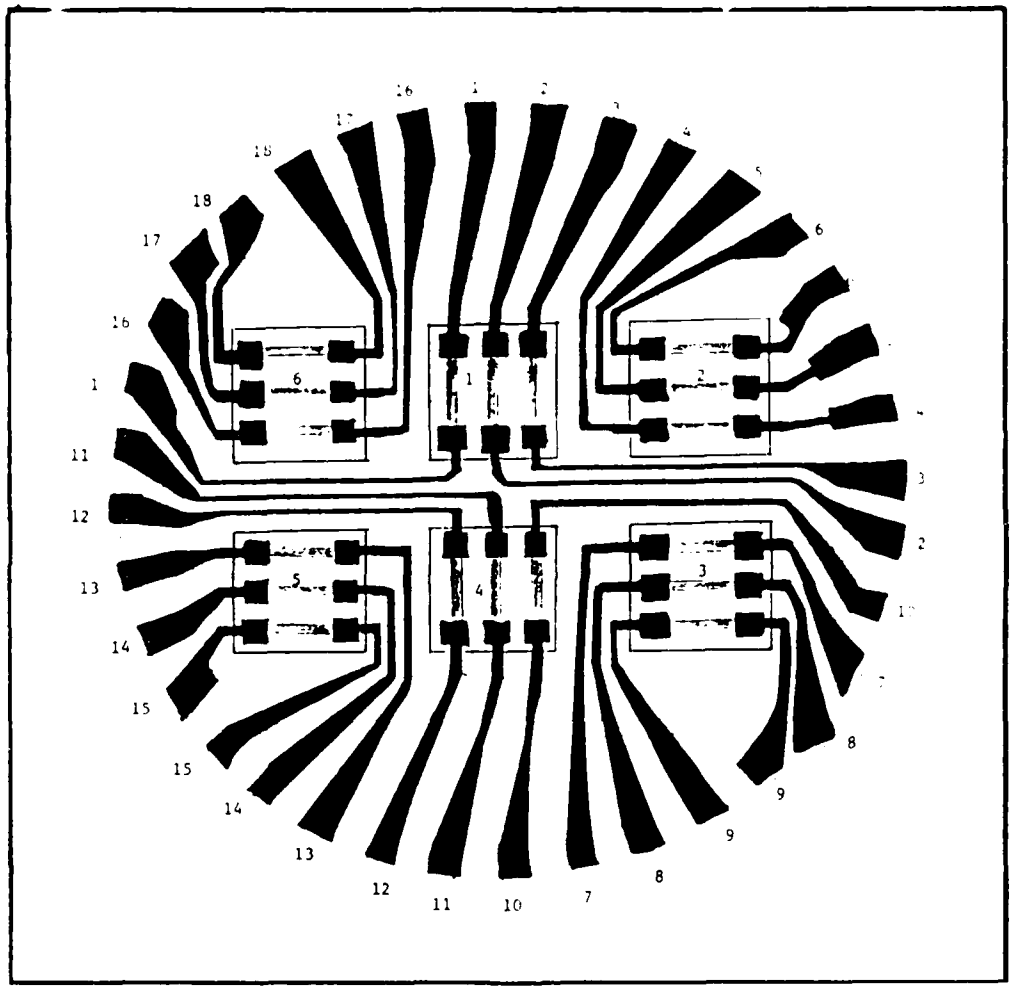


Figure 3-11. Numbering Scheme for the Circuits and Die on the Samples.

degrees relative. The electrical test [illegible] consisted of [illegible] hours of continuous pulsed [illegible] milliamperes peak current.

Experimental Setup. The instrumental attachment for the [illegible] tests is schematically illustrated in Figure 3-1. The contraption consists of a test jig, pulsed current circuitry, and the counter circuits.

Test Jig. The test jig holds the sample stable during the electrical performance test and allows for interchangeable connections to any of the 36 connection pads on a sample. The test board is illustrated in Figure 3-13. The test jig was fabricated with a high temperature resistant material (Phenolic). The sample was taped to the center of the

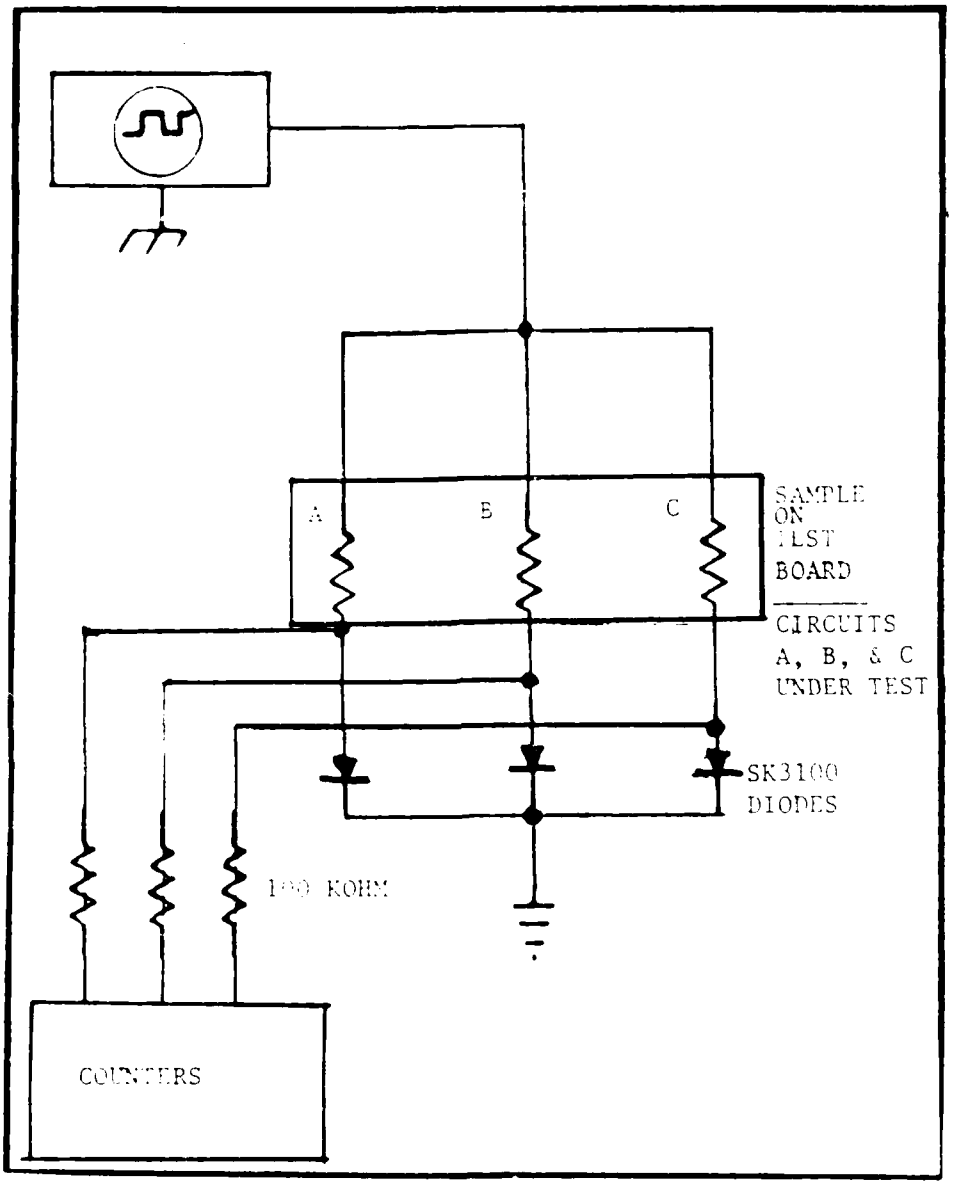

A
B
C
SAMPLE
ON
TEST
BOARD
CIRCUITS
A, B, & C
UNDER TEST
SK3100
DIODES
100 KOHM
COUNTERS

Figure 3-12

AD-A198 482 INVESTIGATION OF A HYBRID WAFER SCALE INTEGRATION TECHNIQUE THAT MOUNTS D (U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI R W MAINGER

2/3

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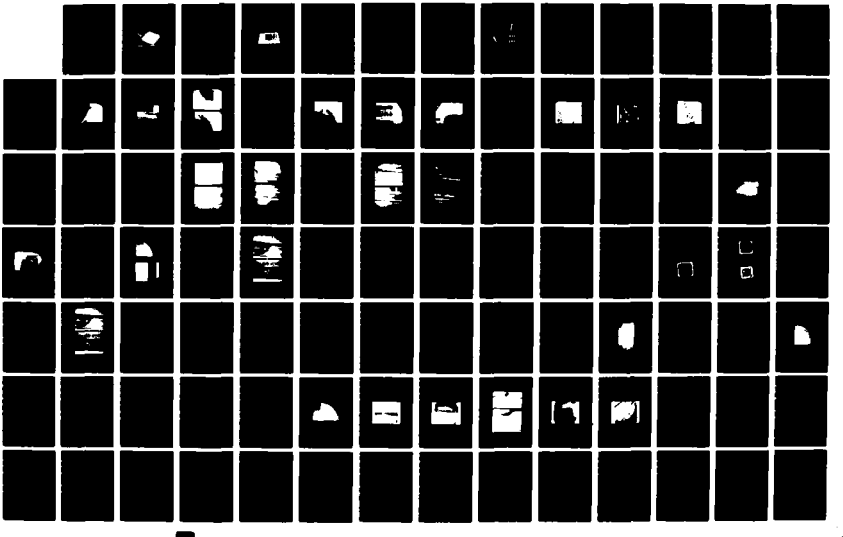
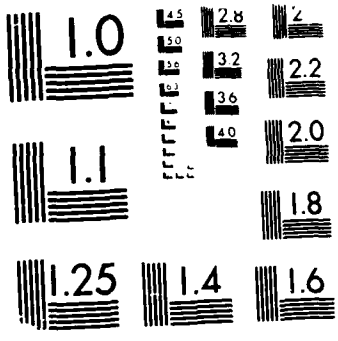




MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

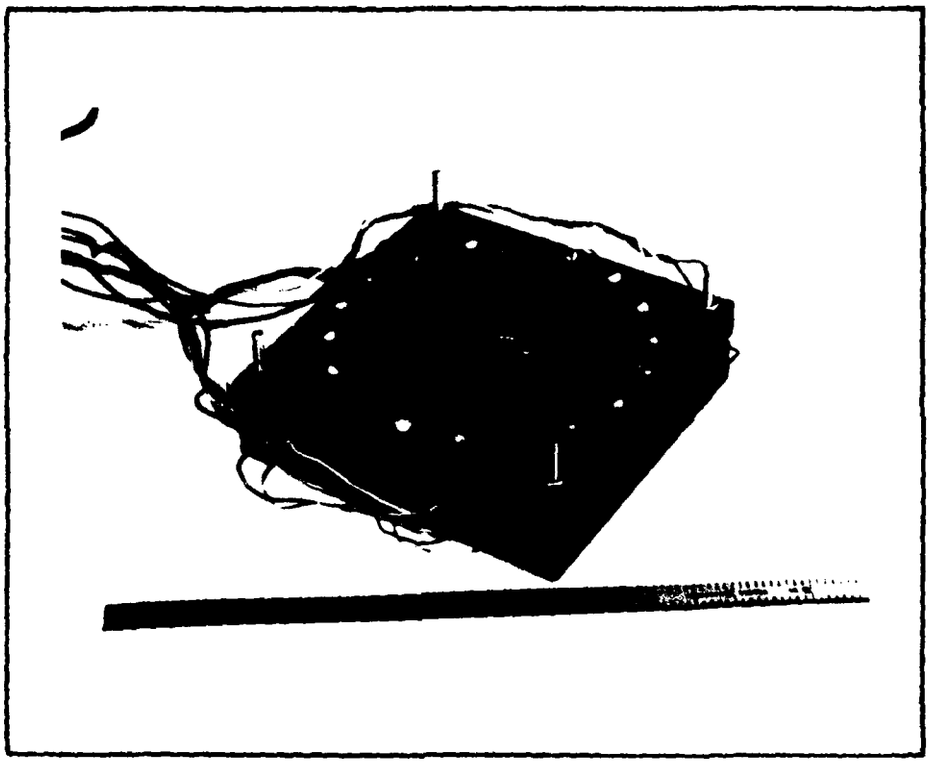


Figure 3-13. Electrical Test Jig.

board with cellophane tape, and the circuits tested were contacted with spring wire leads. Typically, only 3-6 circuits were tested at any given time. The difficulties of placing multiple spring wires onto the pads without scratching them, limited the number of circuits that could be tested in one trial.

Pulsed Current Circuitry. The pulsed current circuitry consisted of the circuit under test (contacted via the test jig) and a signal generator (Model III, Wavetek, Inc., San Diego, CA). Referring to Figure 3-12, a 1 Kilohertz square wave was chosen for the tests. The current through the circuit was controlled by the voltage control on the signal generator. An oscilloscope (Model 575, Tektronix, Inc., Portland, OR) was used to determine the voltage dropped across the resistance of the circuit, and thus, the peak current through the circuit during the pulse which was approximately 50 milliamperes. Up to three circuits on a sample were pulsed to 50 milliamperes each by one signal generator.

Counter Circuits. To determine the precise point in time that a circuit has failed, digital counter circuits were constructed and used to count the pulses passing through the circuit. The counters were isolated from the test circuits with 100 kilo-ohm resistors. These resistors functioned to limit the current flowing into the counter circuits. The counters were simple in design and were constructed on circuit design test boards (Elite Boards, no model number, E & L Instruments, Inc., Derby, CT). The chip-level schematic of a counter circuit is illustrated in Figure H-1 in Appendix H. Two counter circuits were fabricated on an Elite Board. Figure 3-14 illustrates an elite board with two counter circuits.

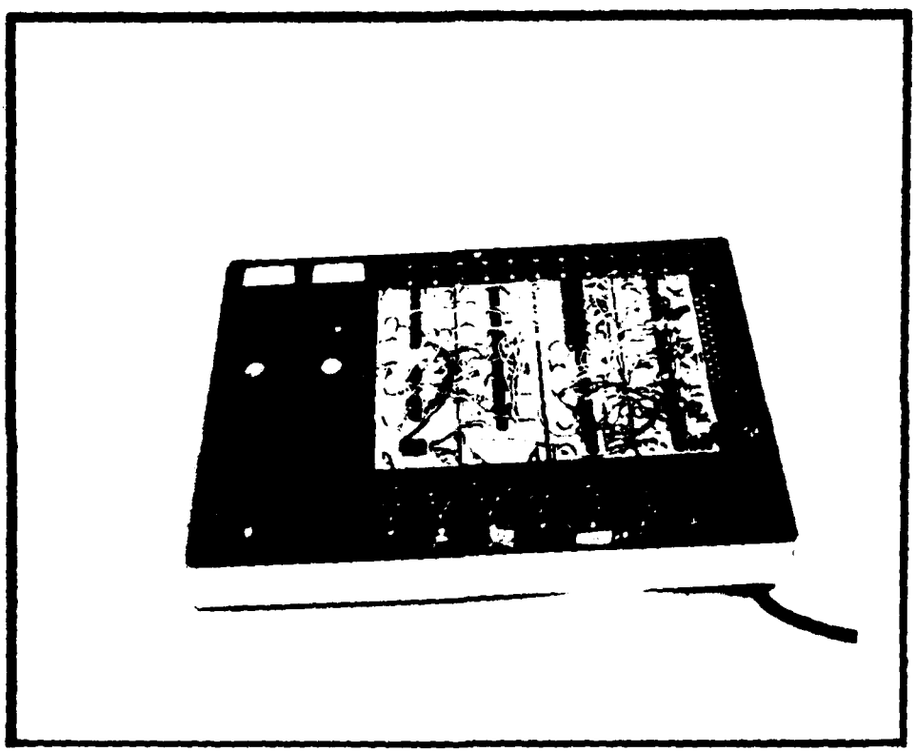


Figure 3-14. Elite Board With Two Counter Circuits.

Room Temperature Test (20 degrees Celsius). All functional circuits were tested for 60 hours at room temperature. The time of failure was recorded for all circuits which stopped conducting during the test. To avoid loss of conduction at the spring wire/pad interface, a small dot of conductive ink (Amicon C-993-34, Amicon, Inc., Lexington, MA) was placed at each interface and cured at 70 degrees Celsius for 20 minutes. Multiple test sessions were conducted for each samples since only 3-6 circuits were tested in any one period.

Elevated Temperature Test (150 degrees Celsius). All functional circuits (the survivors of the room temperature MTTF test) were tested for 60 hours at 150 degrees Celsius. The test board was placed into a convection oven calibrated to 150 degrees Celsius (quartz thermometer). The time of failure was recorded for all circuits which stopped conducting during the test. To avoid loss of conduction at the spring wire/pad interface, a small dot of conductive ink was placed at each interface and cured as in the room temperature test. Again, multiple test sessions were conducted for each sample, since only 3-6 circuits were tested at any one time.

High Temperature Tests. The three tests which exposed the samples to temperatures up to 350 degrees Celsius were called the high temperature tests. These tests sought to determine the effect of high temperature on the polyimide. Earlier temperature test results motivated the limitation of the 250 degree temperature (Chapter IV: Effect of Processing Temperature on Further Process Steps). These tests will evaluate whether further imidization of the polyimide layer will adversely effect the sample.

High Rate of Temperature Increase Test. The purpose of this test was to observe the results of subjecting one sample to a rapid increase in temperature. Sample C was placed on a hotplate heated to 350 degrees Celsius. The sample was thus subjected to rapid heating. The results of this test are reported in Chapter IV.

Ramped Temperature Test. The purpose of this test was to observe the results of gradually heating a sample to a high temperature. Sample A was placed in a forced air oven set at 175 degrees Celsius for 30 minutes, removed, and inspected. The sample was then returned to the oven which had its temperature increased by 25 degrees Celsius. The sample remained under these conditions for 30 minutes, was removed, and then inspected. This routine was repeated until the oven temperature reached the 350 degrees Celsius level. The results of this test are reported in Chapter IV.

High Temperature Endurance Test. The purpose of this test was to determine the results for leaving a gradually heated sample (sample A from the last test) at the 350 degree Celsius point for a period longer than 30 minutes. After sample A had reached the 350 degree Celsius level during the previous test, it was left at that temperature for 16 hours. The sample was removed from the oven at 1, 2, 4, 6, 8, and 16 hours duration and its condition was observed. The results of this test are discussed in Chapter IV.

Fault Analysis of the Final Samples. To evaluate the effectiveness of the overall fabrication process, it is important to understand how the samples failed and how often any particular failure mode occurred.

Possible Faults. There are two key areas where most circuit failures could occur: at the "gap" region where the metal conductor transitions from the surface of the support substrate to the surface of the die, and at the vias. At the transition region, breaks in the aluminum conductor could result in an open circuit. Likewise, vias may not conduct due to steep sloping sidewalls.

Statistical Analysis of Fault Occurrence. Each failed circuit on the three final samples was probed to determine the exact location of the fault. Using the diagram in Figure 3-15 and Table 3-III as a reference, this technique can be described. A digital multimeter was used to check for open circuits. The probes were first placed between points 1 and 2 (Figure 3-15). If the circuit was open (an infinite resistance reading on the meter) between these two points, the conductor was defective and most likely has a break in the metal. This procedure was duplicated for all of the sets of points listed in Table 3-III. The results of the probing led to an understanding of which points on the conductor are most susceptible to defects. The results of this test and the analysis are given in Chapter IV.

Scanning Electron Microscopy of The Faults. Micrographs from the scanning electron microscope (SEM) revealed the characteristic faults found in the final samples. These micrographs are presented in Chapter IV.

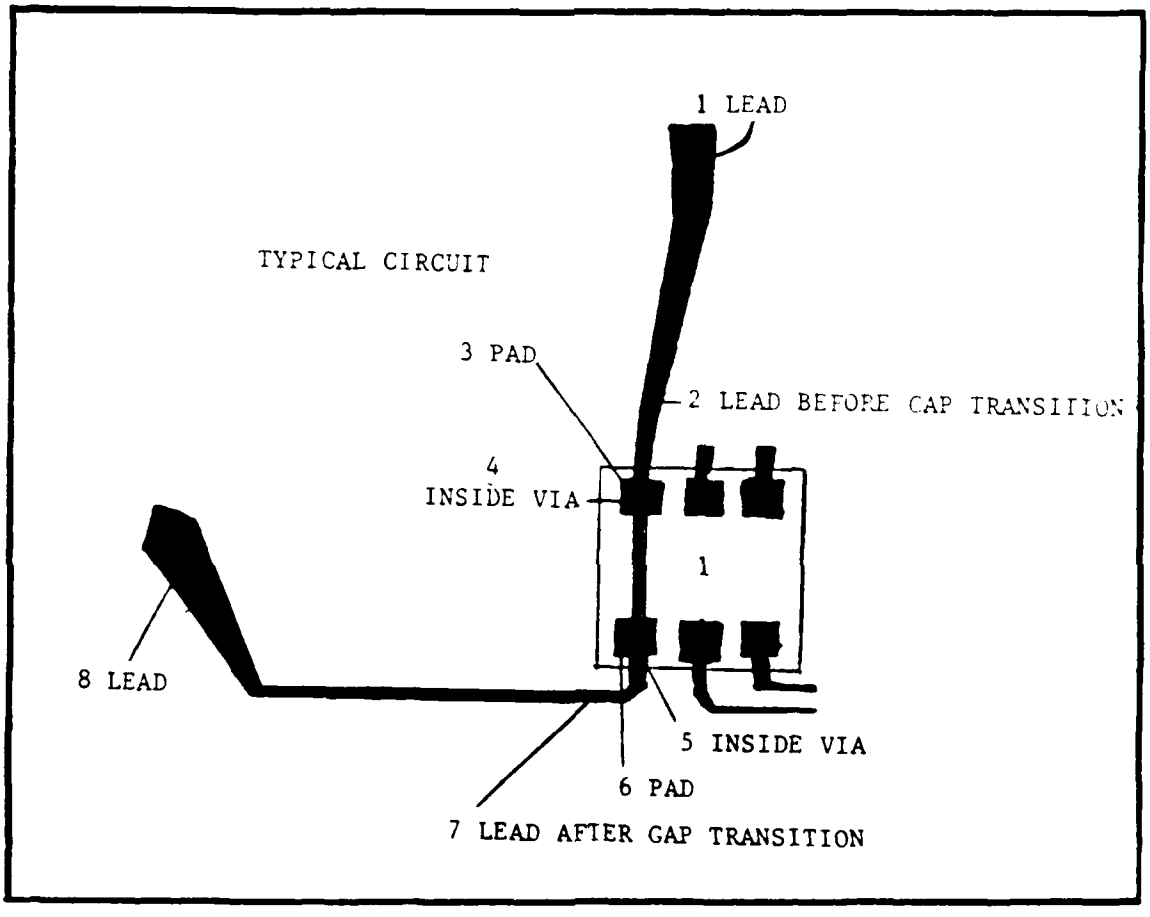


Figure 3-16. Probe Points On Each Circuit.

Table 3-III. Guide to Determining the Location of Conductor Defects.

If an open circuit exists between			
Point	and	Point.	then the fault is located at the:
1		2	1st conductor
2		3	1st transition
3		4	1st via
4		5	IC circuit
5		6	2nd via
6		7	2nd transition
7		8	2nd conductor

IV. Experimental Results And Discussion

This chapter contains the results and a discussion of the experimental procedures described and implemented in Chapter III. The sequence of presentation corresponds to that in Chapter III.

Wet Orientation Dependent Etching Study Results

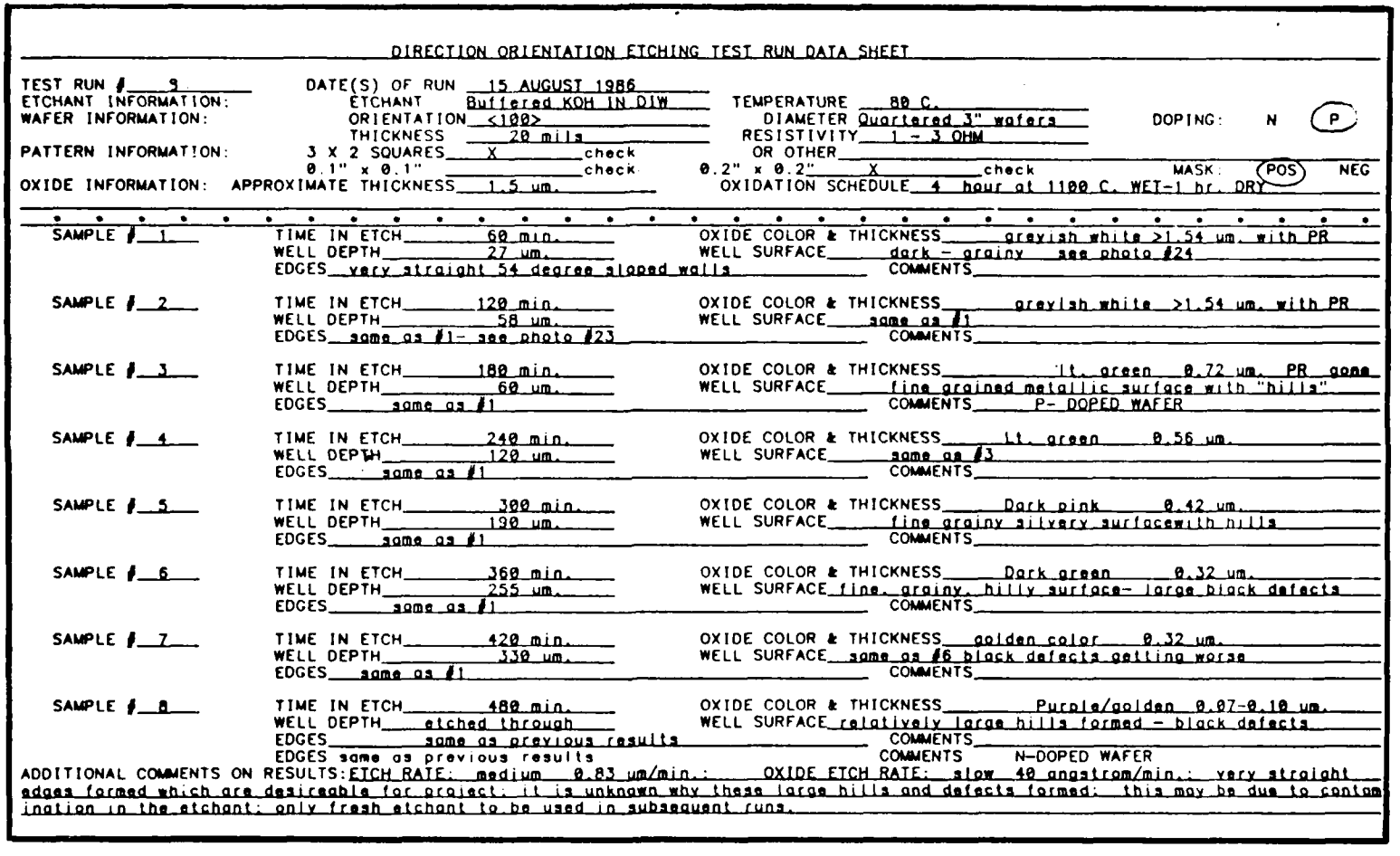
Twelve etch trials were accomplished as indicated in Table 4-I. The objective was to discern the etch characteristics of two silicon wafer crystal orientations combined with the three etchants.

Etching Results. The results of each etch trial are presented on data sheets which are presented in Appendix E. The data sheet of a typical trial is presented in Figure 4-1. Complete information regarding the type of wafer etched, the etchant (chemical composition and temperature), and thickness of the oxide mask are given in the upper portion of the data sheet. The lower section of each data sheet (Figure 4-1) summarizes the results observed at each occurrence (or sampling time) that a sample wafer was removed from the etchant. The depth of the wells, the color of the oxide mask, and the condition of the well's bottom surface was commented on. For example, on trial #9, the (100) oriented silicon wafers were etched in the buffered potassium hydroxide solution at 80 degrees Celsius. The wafer was removed each hour over an eight hour span. At each sampling point, the depth of the wells was measured (optical microscope). The rate at which the silicon was etched is linear and is plotted in Figure 4-2. For trial #9, the etch rate was 0.83 microns per minute. After each of the twelve trials, it was concluded that this etch rate is moderately fast rate compared to the others, and this fact was noted in the comments section of the data

Table 4-I. Matrix of Silicon Wafer and Chemical Etchant Combinations.

		SILICON SUBSTRATES	
		(100) n-and p-DOPED	(110) n-DOPED
ETCHANTS	KOH in DIW	WODE runs #1 & 3	WODE runs #2 & 10
	Buffered KOH in DIW	WODE runs #5, 7, 8, & 9	WODE run #4
	PED in DIW	WODE runs #6 & 12	WODE run #11

Key:
KOH = potassium hydroxide
DIW = deionized water
PED = pyrocatechol ethylenediamine
WODE = wet orientation dependent etching



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 9 DATE(S) OF RUN 15 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER Quartered 3" wafers DOPING: N (P)

THICKNESS 20 mils RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" check 0.2" x 0.2" X check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.5 um. OXIDATION SCHEDULE 4 hour at 1100 C. WET-1 hr. DRY

SAMPLE # 1
TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS greyish white >1.54 um. with PR
WELL DEPTH 27 um. WELL SURFACE dark - grainy see photo #24
EDGES very straight 54 degree sloped walls COMMENTS

SAMPLE # 2
TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS greyish white >1.54 um. with PR
WELL DEPTH 58 um. WELL SURFACE same as #1
EDGES same as #1- see photo #23 COMMENTS

SAMPLE # 3
TIME IN ETCH 180 min. OXIDE COLOR & THICKNESS lt. green 0.72 um. PR gone
WELL DEPTH 60 um. WELL SURFACE fine grained metallic surface with "hills"
EDGES same as #1 COMMENTS P- DOPED WAFER

SAMPLE # 4
TIME IN ETCH 240 min. OXIDE COLOR & THICKNESS lt. green 0.56 um.
WELL DEPTH 120 um. WELL SURFACE same as #3
EDGES same as #1 COMMENTS

SAMPLE # 5
TIME IN ETCH 300 min. OXIDE COLOR & THICKNESS Dark pink 0.42 um.
WELL DEPTH 190 um. WELL SURFACE fine grainy silvery surfacewith hills
EDGES same as #1 COMMENTS

SAMPLE # 6
TIME IN ETCH 360 min. OXIDE COLOR & THICKNESS Dark green 0.32 um.
WELL DEPTH 255 um. WELL SURFACE fine, grainy, hilly surface- large black defects
EDGES same as #1 COMMENTS

SAMPLE # 7
TIME IN ETCH 420 min. OXIDE COLOR & THICKNESS golden color 0.32 um.
WELL DEPTH 330 um. WELL SURFACE same as #6 black defects getting worse
EDGES same as #1 COMMENTS

SAMPLE # 8
TIME IN ETCH 480 min. OXIDE COLOR & THICKNESS Purple/golden 0.07-0.10 um.
WELL DEPTH etched through WELL SURFACE relatively large hills formed - black defects
EDGES same as previous results COMMENTS
EDGES same as previous results COMMENTS N-DOPED WAFER

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.83 um/min.; OXIDE ETCH RATE: slow 40 angstrom/min.; very straight edges formed which are desireable for project; it is unknown why these large hills and defects formed; this may be due to contamination in the etchant; only fresh etchant to be used in subsequent runs.

Figure 4-1. Typical Wet Orientation Dependent Etching Study Data Sheet. (Trial #9 is featured in illustration.)

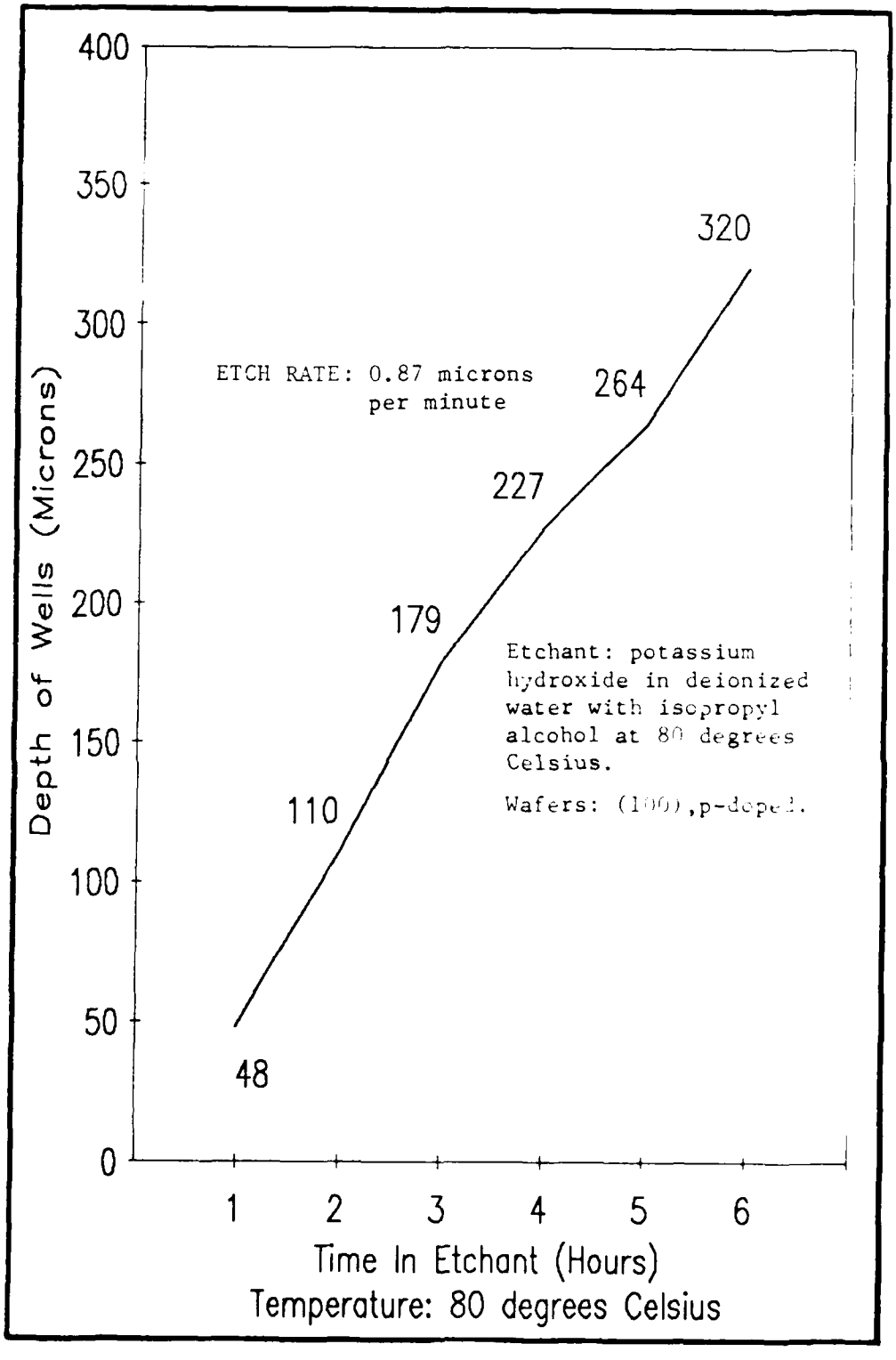


Figure 4-2. Plot of Well Depth Versus Time in the Etchant. Etchant: buffered potassium hydroxide in deionized water at 80 degrees Celsius (Trial #9).

sheet. The etch rate of the oxide mask was observed by noting the color of the oxide and comparing it to a standard oxide color chart. From the chart, the oxide thickness can be estimated and the rate of oxide removal calculated. Finally, the well's bottom surface condition was observed, and comments are recorded on the appropriate line. Optical microphotography was accomplished to document the condition of a well's bottom surface.

Results of Etching (100) Silicon. Eight trials (1, 3, 5, 6, 7, 8, 9, and 12) were conducted using (100) wafers. Using a square well mask, the etched (100) wafers yielded straight edged wells with smooth sloping sidewalls, as illustrated in Figure 4-3. The sidewalls angle at approximately 50 degrees with respect to the plane containing the well's bottom. This angle is shown in Figure 4-4. This result yielded an opening at the top of the well larger than the well's bottom surface. Simple trigonometry revealed that the well's top surface opening is (2d / tan θ) wider compared to the well's bottom (d is the depth of the well and θ is the angle of the sidewall. These variables are illustrated in Figure 4-4.). If the well was etched to a 300 micron depth and the angle θ is 50 degrees, then the well is [(2 x 300)/ tan 50 degrees] 503 microns (19.8 mils) wider at the top of the well. This means that with 300 micron (or about 12 mils) well depths, and if the die size is matched to the size of the well's bottom, there will be approximately a 10 mil "gap" surrounding the die.

Etching with 45% by weight KOH in DIW (without isopropyl alcohol) yielded a rough, uneven well bottom (Figures 4-3 and 4-5). The other two etchants yielded smooth well bottoms. The buffered KOH in DIW

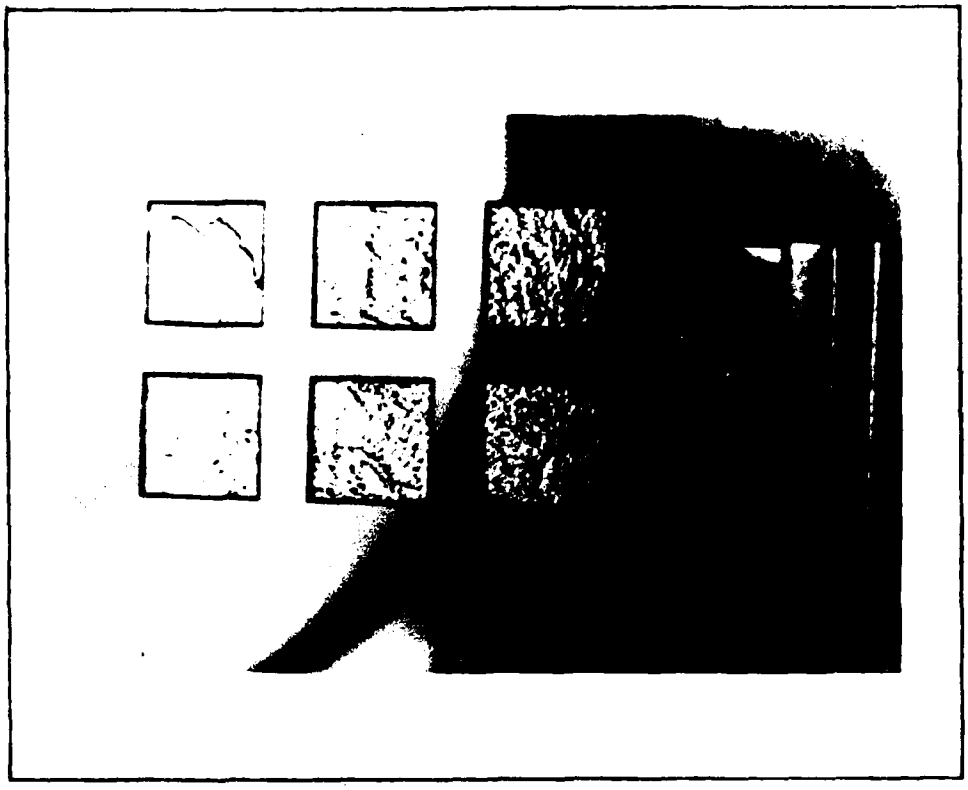


Figure 4-3. Typical Result of Etching (100) Silicon. With all three etchants, (100) silicon consistently yielded precisely square wells with angled sidewalls. The rough well bottoms resulted from using the 45% (by weight) potassium hydroxide in deionized water etchant at 80 degrees Celsius (Trial #3). The magnification factor is 3X.

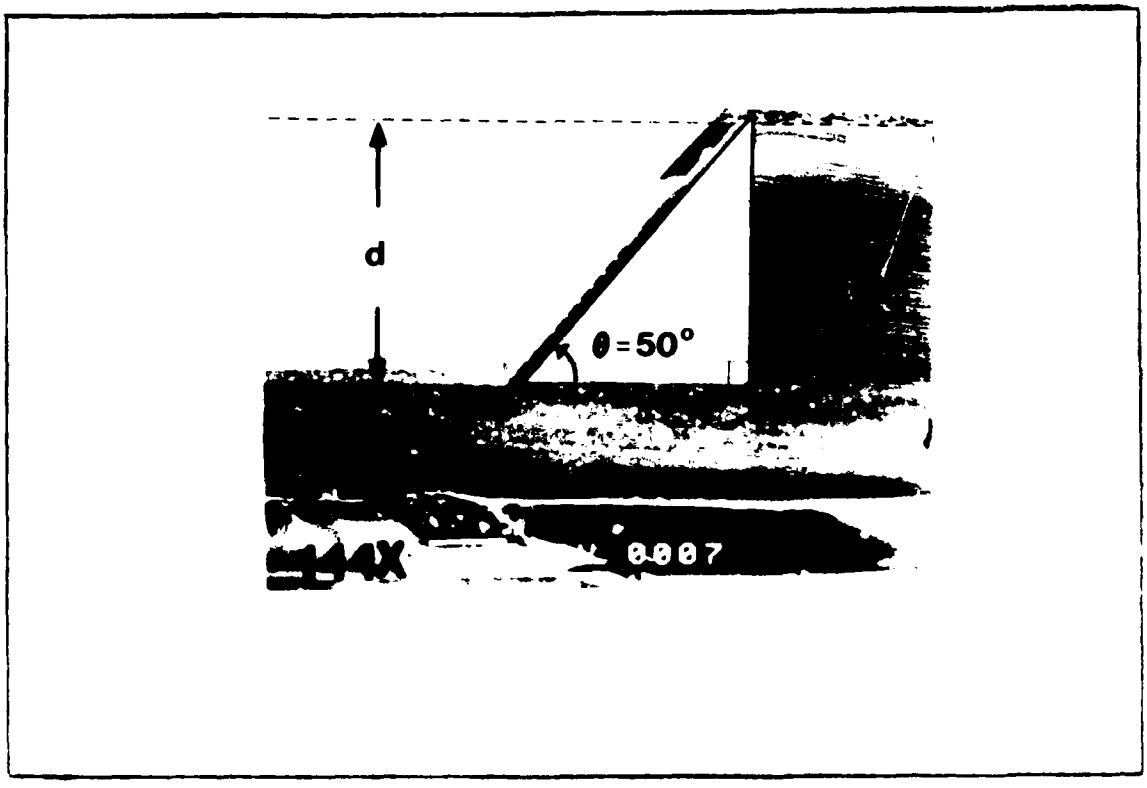


Figure 4-4. Sidewalls Resulting From Etching (100) Silicon. The angle theta is 50 degrees. Depth d of the well is 245 microns (9.6 mils). Wafer thickness is 340 microns. Etchant: Buffered potassium hydroxide in deionized water at 80 degrees Celsius (Trial #9). The magnification factor is 144X.

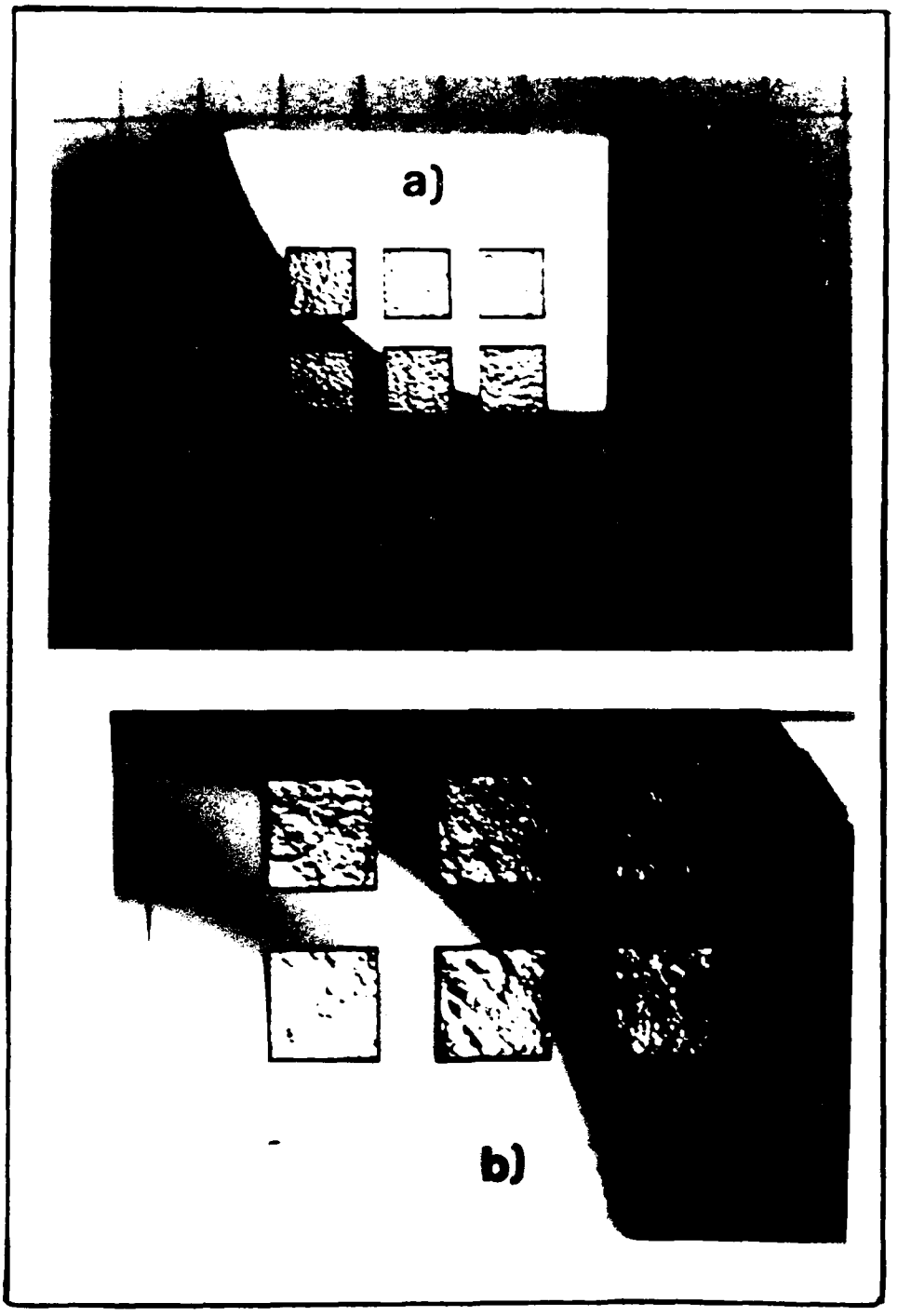


Figure 4-5. Rough Well Surfaces Characteristic of Etching (100) Silicon With 45% (by weight) Potassium Hydroxide in Deionized Water. a) Full wafer view; the magnification factor is 1.8X and b) Closeup view; the magnification factor is 3.0X (Trial #3).

(with isopropyl alcohol) at 80 degrees Celsius, yielded well bottom surfaces which were very smooth. Several of the well bottom surfaces were mirror-like in appearance. An example of this situation is illustrated in Figure 4-6. The wafers etched with the PED and DIW solution (at 100 degrees Celsius) had well bottom surfaces which were finely grained and very even, as illustrated in Figure 4-7. There was no observed etching characteristic differences between p-doped and n-doped (100) wafers.

Results of Etching (110) Silicon. Four trials (2, 4, 10, and 11) were conducted using (110) wafers. The results associated with using this orientation were generally consistent, regardless of the etchant. The two sidewalls parallel to the wafer flat (care was taken to align the mask to the flat to within a $\pm$ 0.5 degree accuracy as discussed in Chapter II) form sidewalls which are perpendicular to the planes containing the well's top and bottom surfaces. This is a very desirable etching trait because it reduces the "gap" encountered when the (100) silicon wafers were etched. However, the other two edges etch outward forming slightly rhomboid shapes. This outward etching is illustrated in Figure 4-8. The undercut areas form planes which are angled approximately 35 degrees with respect to the plane containing the well's bottom. The 35 degree angle was verified by measuring the depth of the well and the width of the undercut area. The angle is the inverse tangent of the ratio of the well's depth to the width of the undercut region. The gray-colored region on Figure 4-8 is the oxide mask that remains intact after the anisotropic etching process. The edges of the well are indicated by the letters (a) and (b).

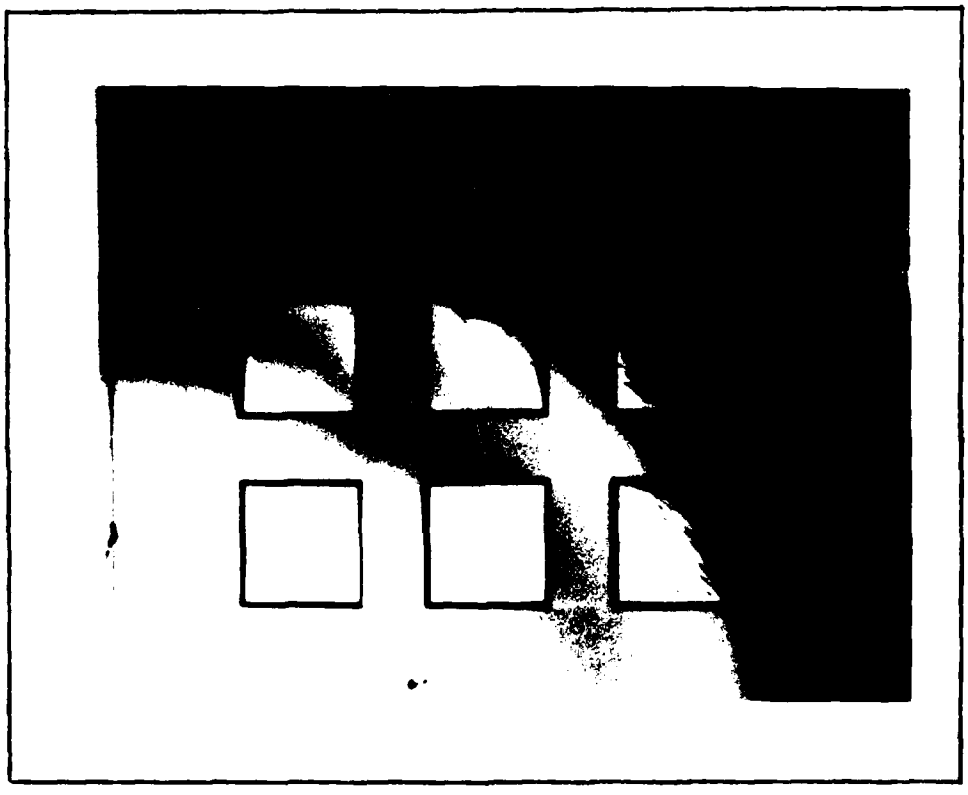


Figure 4-6. Bottom Well Surfaces Characteristic of Etching (100) Silicon With Buffered Potassium Hydroxide in Deionized Water. The well surfaces are mirrorlike (Trial # 9). The magnification factor is 3X.

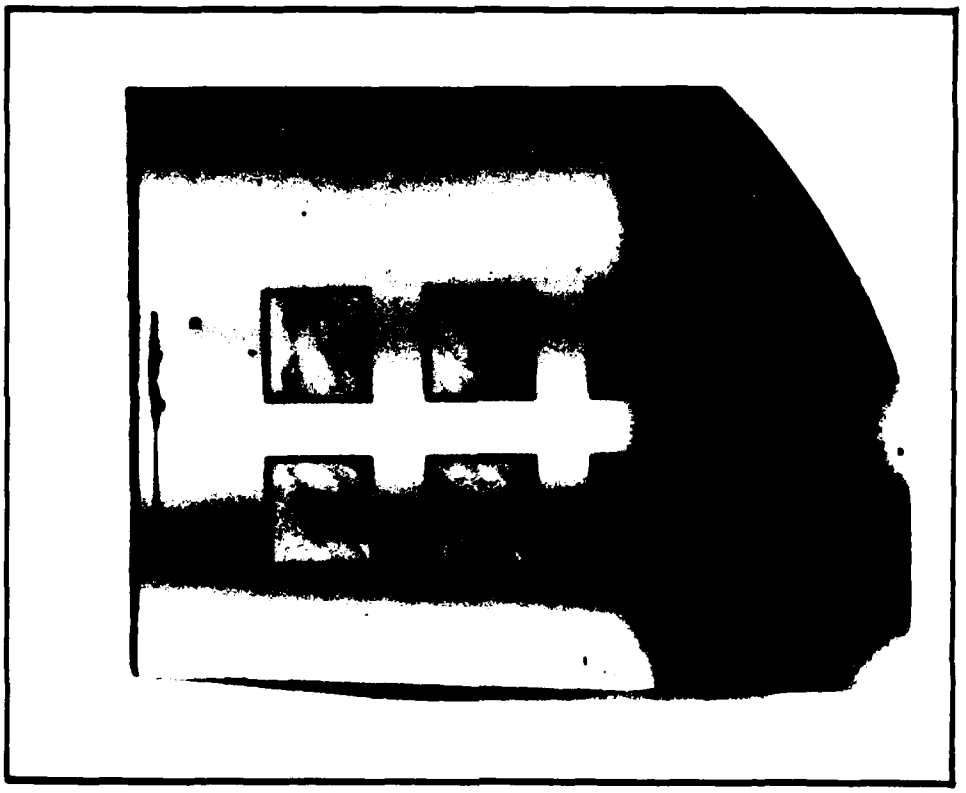


Figure 4-7. Well Surfaces Characteristic of Etching (100) Silicon With the Pyrocatechol Ethylenediamine Etchant. The well surfaces are smooth and have a fine grainy texture (Trial #12). Arrows point to etching defects. The magnification factor is 3X.

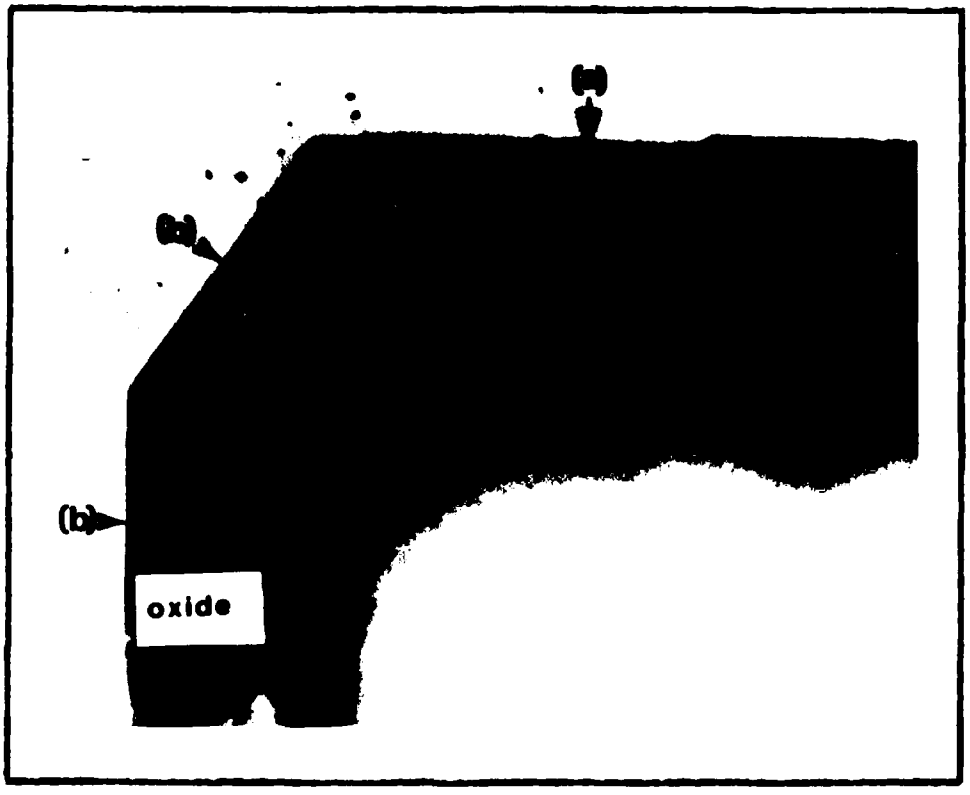


Figure 4-8. Typical Results of Etching (110) Silicon.
The edge (a) is nearly vertical while the edge (b) is sloped at a 35 degree angle. Photograph illustrates the rhomboid shape of the well (Trial #2). The magnification factor is 375X.

Unsuitable well bottoms formed from etching with this orientation type. The 45% (by weight) KOH in DIW etchant produces a rough and uneven well bottom very similar to that found when etching (100) wafers with this etchant (Figure 4-9). The left edge of the sample shown in Figure 4-9 is the magnified undercut edge of Figure 4-8. Both the buffered KOH and PED etchants yielded well bottoms with severe striations or groove-like defects which would not be suitable to bond die to. The striations differ in height, and therefore, the surface is uneven. Figure 4-10 illustrates the corner of one well etched into (110) silicon and shows both the rhomboid shape of the resulting wells and the striations on the well's bottom. This result is typical for both of these etchants.

Results of Etching With KOH in DIW. Four trials (1, 2, 3, and 10) were conducted using the 45% (by weight) KOH in DIW etchant and the results were consistently poor. The oxide masks etched at a rapid rate, necessitating thick oxide masks. The etchant yielded well bottom surfaces in both silicon types which were rough and uneven (Figures 4-3, 4-5, and 4-9).

Results of Etching With Buffered KOH in DIW. Five trials (4, 5, 7, 8, and 9) were conducted using this etchant. Favorable results were achieved using (100) silicon. The etchant produced flat, fine grained well bottoms that were realized with moderate silicon etch rates and slow oxide etch rates. These results are illustrated in Figure 4-6. Poor results were obtained using (110) silicon; the well bottoms were heavily striated, as seen in Figure 4-10.

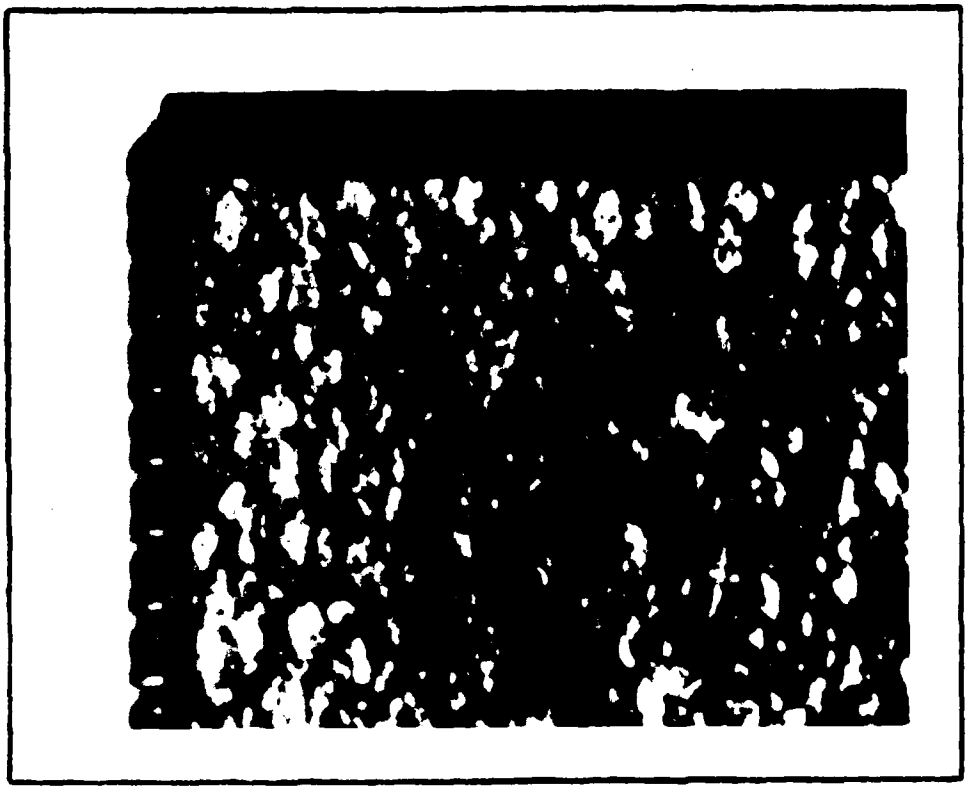


Figure 4-9. Corner of a Well Etched Into (110) Silicon. The well's bottom surface is very rough. The etchant was 45% (by weight) potassium hydroxide in de-ionized water at 80 degrees Celsius (Trial #2). The magnification factor is 75X.

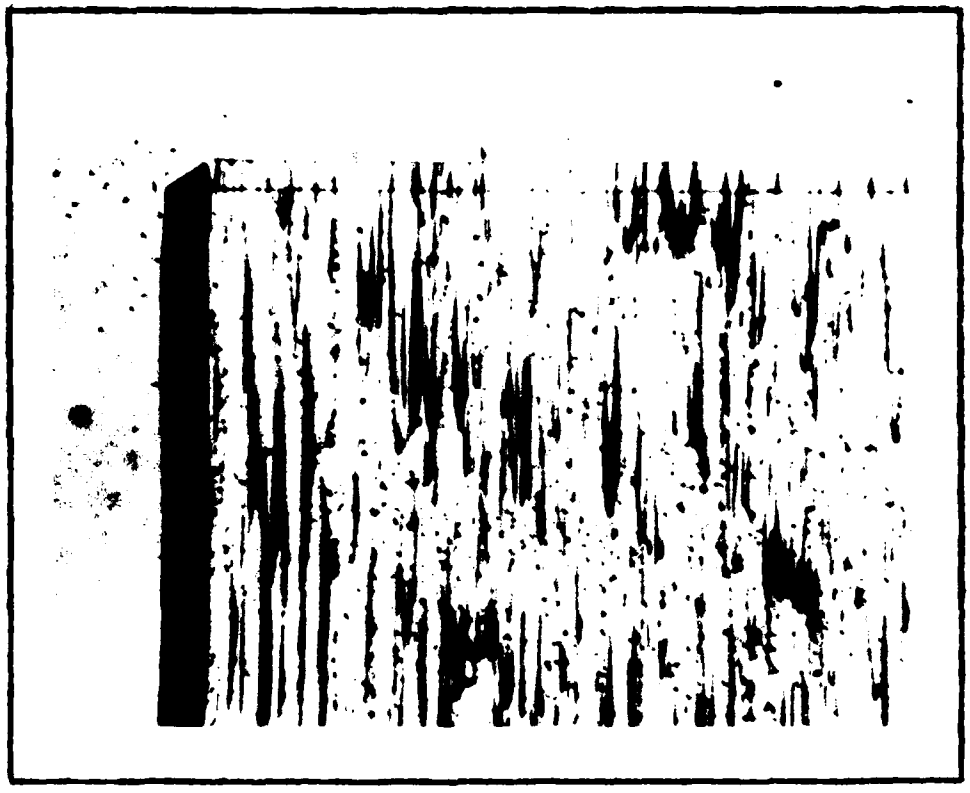


Figure 4-10. Corner of a Well Etched Into (110) Silicon. The well's bottom is severely striated. The etchant is buffered potassium hydroxide in deionized water at 80 degrees Celsius (trial #4). The magnification factor is 75X.

Figure 4-11. Etching Residue Left After Etching (100) Silicon With the Pyrocatechol Ethylenediamine Etchant. The etchant temperature was 100 degrees Celsius (Trial #12). The magnification factor is 375X.

Table 4-II. Results of Wet Orientation Dependent Etching Study.

ETCHANTS		SILICON SUBSTRATES: (100) n-and p-DOPED	SILICON SUBSTRATES: (110) n-DOPED
	KOH in DIW	TRIALS #1 and #3 Etch rate: medium/slow 0.75 um /min Oxide etch: Too fast 400 Angstroms/min Edges: Beveled 54 degrees Surface: uneven, grainy NOT RECOMMENDED	TRIALS #2 and #10 Ftch rate: Good 1.6 um /min Oxide etch: Too fast 400 Angstroms/min Edges: ragged Surface: rough NOT RECOMMENDED
	Buffered KOH in DIW	TRIALS #5, #7, #8, & #9 Etch rate: medium 0.9 um /min Oxide etch: slow 40 Angstroms/min Edges: very straight beveled at 54 degrees Surface: mirrorlike RECOMMENDED	TRIAL #4 Etch rate: slow 0.5 um /min Oxide etch: slow 44 Angstroms/min Edges: undercutting beveled at 35 degrees Surface: striations rhomboid formation NOT RECOMMENDED
	PED in DIW	TRIALS #6 and #12 Etch rate:medium to fast 1.1 um /min Oxide etch:very slow 8 Angstroms/min Edges: very straight beveled at 54 degrees Surface: fine grainy Residue defects at edges NOT RECOMMENDED	TRIAL #11 Etch rate: medium 0.7 um /min Oxide etch: very slow 8 Angstroms/min Edges: undercutting beveled at 35 degrees Surface: striations NOT RECOMMENDED

Key: KOH - potassium hydroxide
DIW - deionized water
PED - pyrocatechol ethylenediamine
WODE - wet orientation dependent etching

of time needed to etch a batch of wafers.

The etchant will also need to etch the silicon dioxide mask at a very slow rate. Oxide masks up to 2.5 microns can be practically grown for this study. The typical etching time required to etch the support substrates will be on the order of 200-300 minutes. Therefore, the oxide etch rate should be less than 85 Angstroms per minute.

The etching process should form sharply defined wells with straight edges and fairly horizontal sidewalls. Since the mask pattern contains six 200 mil x 200 mil squares in a 3 x 2 pattern, the resulting well pattern must be identical to this pattern. The well shapes must be square at the top and bottom. The spacing between the wells should be retained as this will be the area where the circuit interconnects will be accomplished.

The surface of the well bottoms should be uniform and relatively smooth. To promote physical adhesion for die bonding, the surface should be smooth, or at worst, slightly grainy. No gross defects (such as etching residues or striations) should be present as they will interfere with bonding the die to the well.

Discussion of the Results. The matrix of etchant and silicon wafer combinations (Table 4-II) is a convenient way to summarize the strengths and weaknesses of each choice.

The (110) orientation combinations did not show promise for this project. Consistently, two of the four edges on each well would form fairly vertical sidewalls. It was observed that, unless the flat and mask were precisely aligned (the literature indicates a tolerance of $\pm$ 0.25 degrees), these two sidewalls would be ragged and not have a

straight clean edge at the top of the well. The other two sidewalls consistently etch under the oxide mask at a 35 degree angle with respect to the top surface. This undercutting causes the wells to form in rhomboid shapes as shown in Figures 4-8, 4-9, and 4-10. In two of the (110) combinations (KOH-DIW-IPA and PED-DIW), deep striations formed on the well's bottom surface. These grooves would be poor surfaces to bond to because they are uneven. Additionally, according to the literature (12:1178), (110) wafers are of poor crystalline quality and are expensive and difficult to obtain. For these basic reasons, the combinations involving (110) silicon are rejected.

The results establish that two combinations of anisotropic etchants and silicon wafers are superior to the other four: the buffered KOH in DIW with (100) wafers, and the PED in DIW with (100) wafers. Both combinations use (100) silicon which yields square well shapes. The sidewalls, however, do not form at the ideal 90 degree angle. The etching stops at the (111) plane which forms sidewalls which are angled 50 to 55 degrees with respect to the plane of the well's bottom. Both etchants yield medium silicon etch rates, slow oxide etch rates, and the ability to render uniformly smooth or slightly grainy well surfaces. However, there are advantages to using the KOH etchant compared to the PED etchant. The PED etch frequently leaves a residue defect along the edges of the well. Under the optical microscope, this material appears to be a residue of the etch. However, after attempts to remove the material using buffered hydrofluoric acid and a 10:1 DIW:HF solution, the residue was not removed. This residue is illustrated in Figure 4-11.

Recommendation. It is recommended that the combination of (100) silicon and the buffered KOH in deionized water etchant be used to fabricate the final samples. It is further recommended that quartered 3-inch, n-doped wafers be used as the substrate material. These wafers are recommended because of their thickness (17-22 mils), dopant level (only mildly n-doped), and the fact that they are readily available. After the final samples were evaluated, a recommendation will be made in Chapter V as to whether or not this combination is suitable for the HWSI process.

Die Attach Adhesive Study Results.

Seven die attach adhesives were tested for suitability in bonding discrete die into the wells etched in the WODE study. The results are given in the next section.

Study Results. A discussion of the DAA study is given. The results of bonding with the three gold eutectic materials are presented together; the organic adhesives are discussed individually.

Gold Eutectic Materials. None of the three eutectic alloys formed the desired bond between the die and substrate. A multitude of variations of the procedure were attempted to achieve successful results, including repeating procedures with a focus on increased cleanliness and using ultrasonic vibration. However, successful bonds were not formed.

Dynaloy SM-200 Epoxy. The Dynaloy SM-200 epoxy was easy to apply, and it passed the pry test described in Chapter III. The epoxy's low cure temperature is one of its primary advantages. The SEM photographs are characteristic of the bonds obtained using the Dynaloy adhesive. The bond appears to be firm but displays a "swiss cheese "

effect (shown in Figure 4-12). However, the high frequency of voids will likely cause hot spots to form when the IC is operating.

Amicon ME-990 Epoxy. The Amicon ME-990 epoxy was easy to apply, and it passed the pry test described in Chapter III. It also has a low cure temperature. The SEM photographs (Figure 4-13) are representative of the results found. The adhesive provided regions of homogeneous bonding, as illustrated in Figure 4-13(a). However, there were also areas of large, hollow cavities that formed near the edges of the die, which would also likely yield unacceptable hot spots under functional ICs in Figure 4-13(b). These cavities probably were not due to the application method. Care was taken to coat both the well and backside of the die, as well as providing a matrix of adhesive dots. Most likely, the large voids or cavities form as the adhesive shrinks during cure. This shrinking action causes the adhesive to cluster in the center of the bond leaving some of the edges without adhesive.

Master Bond EP-34CA Special Epoxy. Due to the necessity of mixing the Master Bond epoxy and the resulting viscious mixture produced, it was slightly more difficult to apply compared to the single-component epoxies. This disadvantage, however, was not an insurmountable problem. One advantage of the Master Bond epoxy compared to the single-component epoxies was that once it was mixed, it had a shelf life of over 24 hours. (Single component epoxies should be kept frozen until just before use, and the useful life after thaw is limited to a few hours.) The Master Bond epoxy yielded a good bond which passed the pry test described in Chapter III. SEM micrographs of the bonds revealed that the epoxy produced a thick, homogeneous bond with several

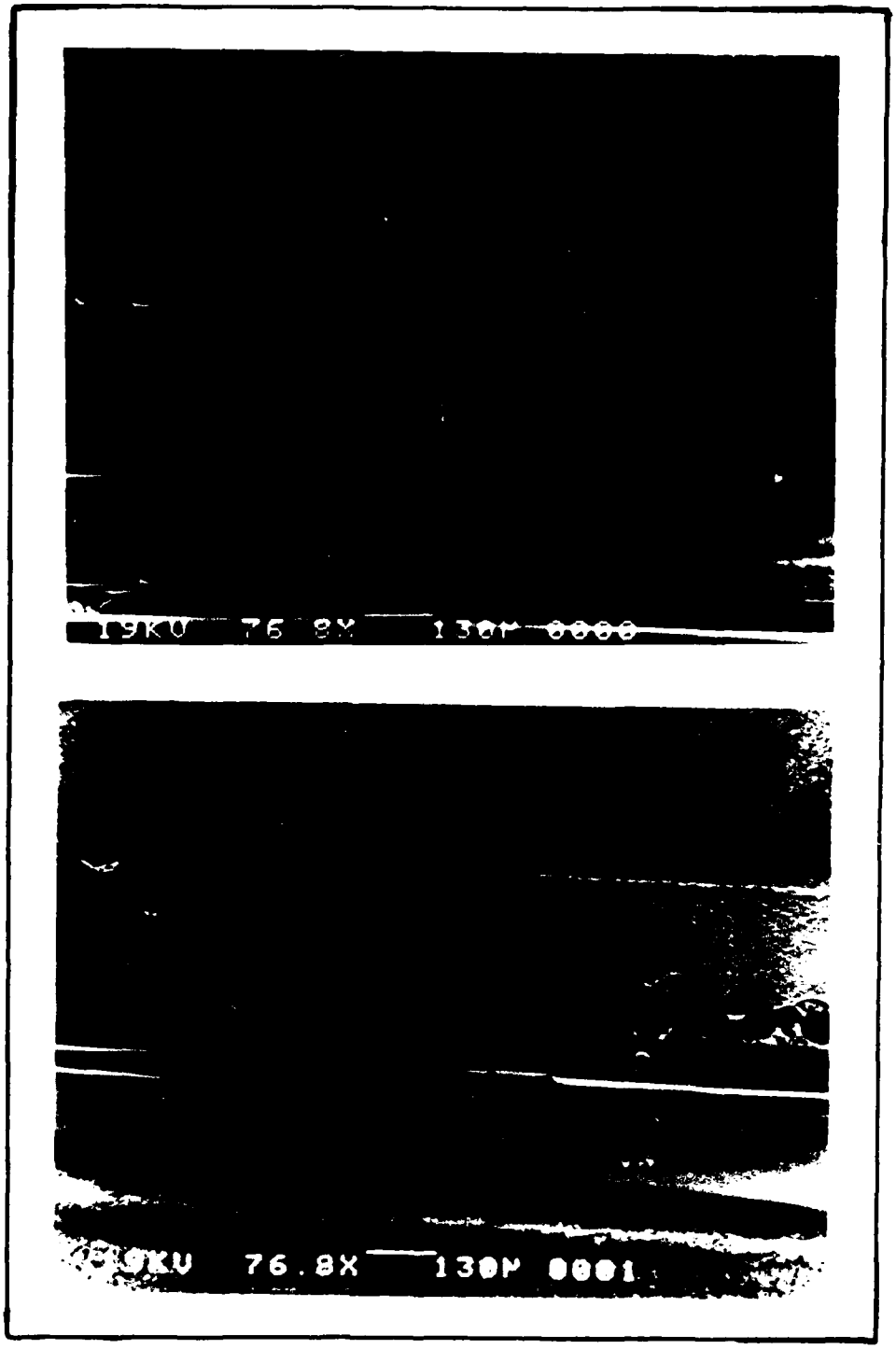


Figure 4-12. Typical Results of Bonding Die in the Wells With Dynaloy SM-200 Epoxy. Both top and bottom photographs illustrate the "swiss cheese" condition of the adhesive layer after cure. The magnification factor of both photographs is 76.8X.

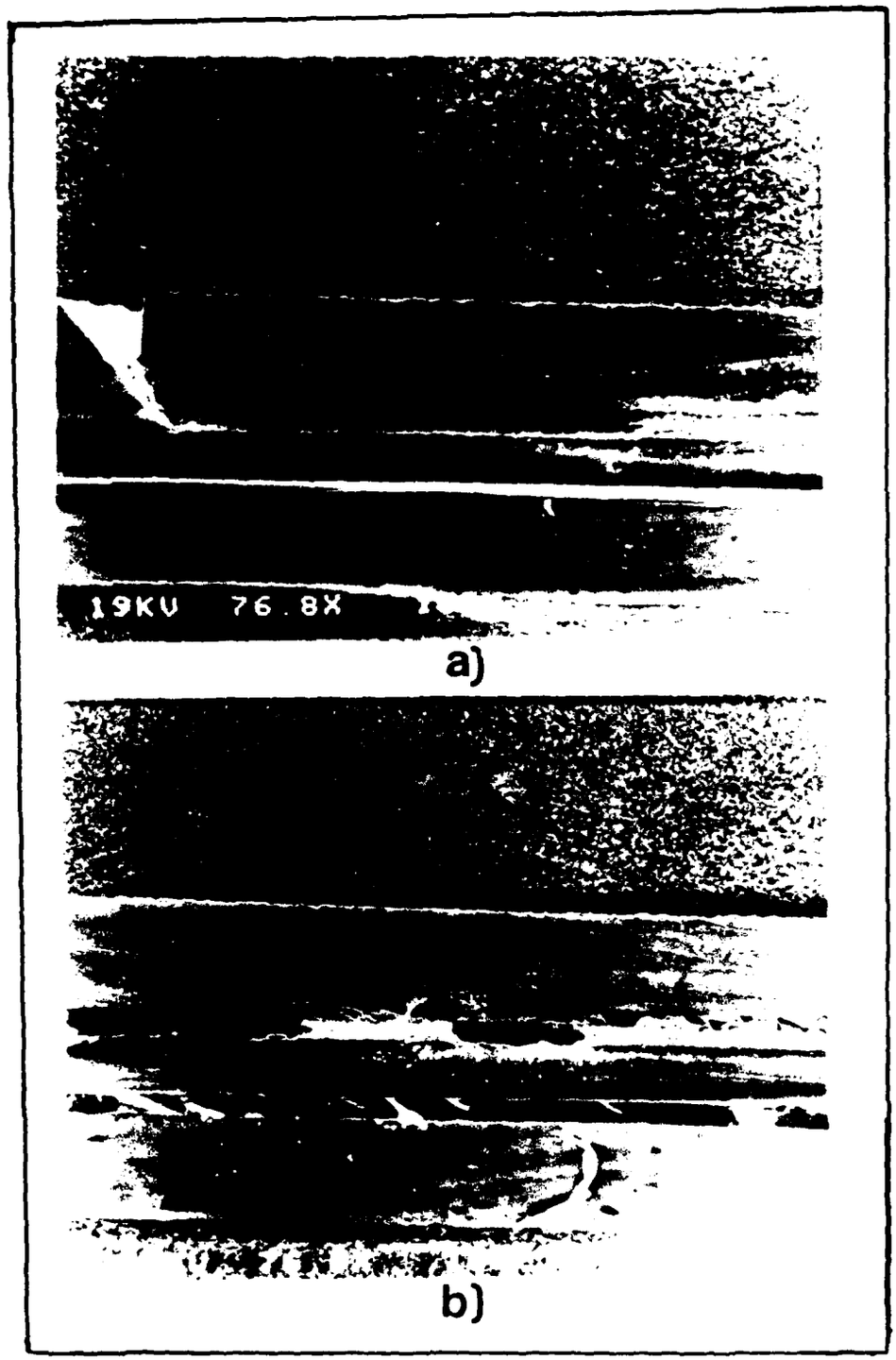


Figure 4-13. Typical Results of Bonding Die in the Wells With Amicon ME-990 Epoxy. a) Adhesive could provide areas of voidless bonding. b) Generally, under the center of the die, large voids formed. The magnification factor of both photographs is 76.8X.

large voids. The photographs in Figure 4-14 illustrate the relative size and frequency of voids.

Quantum Materials QMI-2414 Silver Glass Epoxy. The QMI-2414 silver glass epoxy was easy to apply and yielded a good bond (probably passing the pry test described in Chapter III). The SEM photographs revealed that thin, homogeneous bonds were formed many times without voiding, as characterized by the top photograph of Figure 4-15. However, at the centers of many of the die, a large void formed, as illustrated in the bottom photograph of Figure 4-15.

Summary of Die Attach Adhesive Study Results. A summary chart of the results of the DAA study is given in Table 4-III.

Discussion of the Results of the Die Attach Adhesive Study. The die attach study sought to determine which of the seven standard die attach adhesives were superior for bonding large die within the well structures. The criteria used for making this choice is presented in the next section, followed by a discussion of how each material satisfied the criteria. An optimal choice is recommended.

Criteria for Selecting a Die Attach Adhesive. The obvious criteria for selecting a suitable die attach adhesive was that it must be capable of providing strong bonds. Furthermore, the ideal candidate would have a cure or processing temperature below 250 degrees Celsius, be relatively easy to apply, and have a thermal coefficient of expansion comparably close to that of silicon. Inherent to the criteria of a strong bond is the requirement that the adhesive be relatively free of large and frequent voids. The frequency and type of voids for each adhesive was observed in the DAA study, and the results of this observation constitute the major factor considered in selecting an

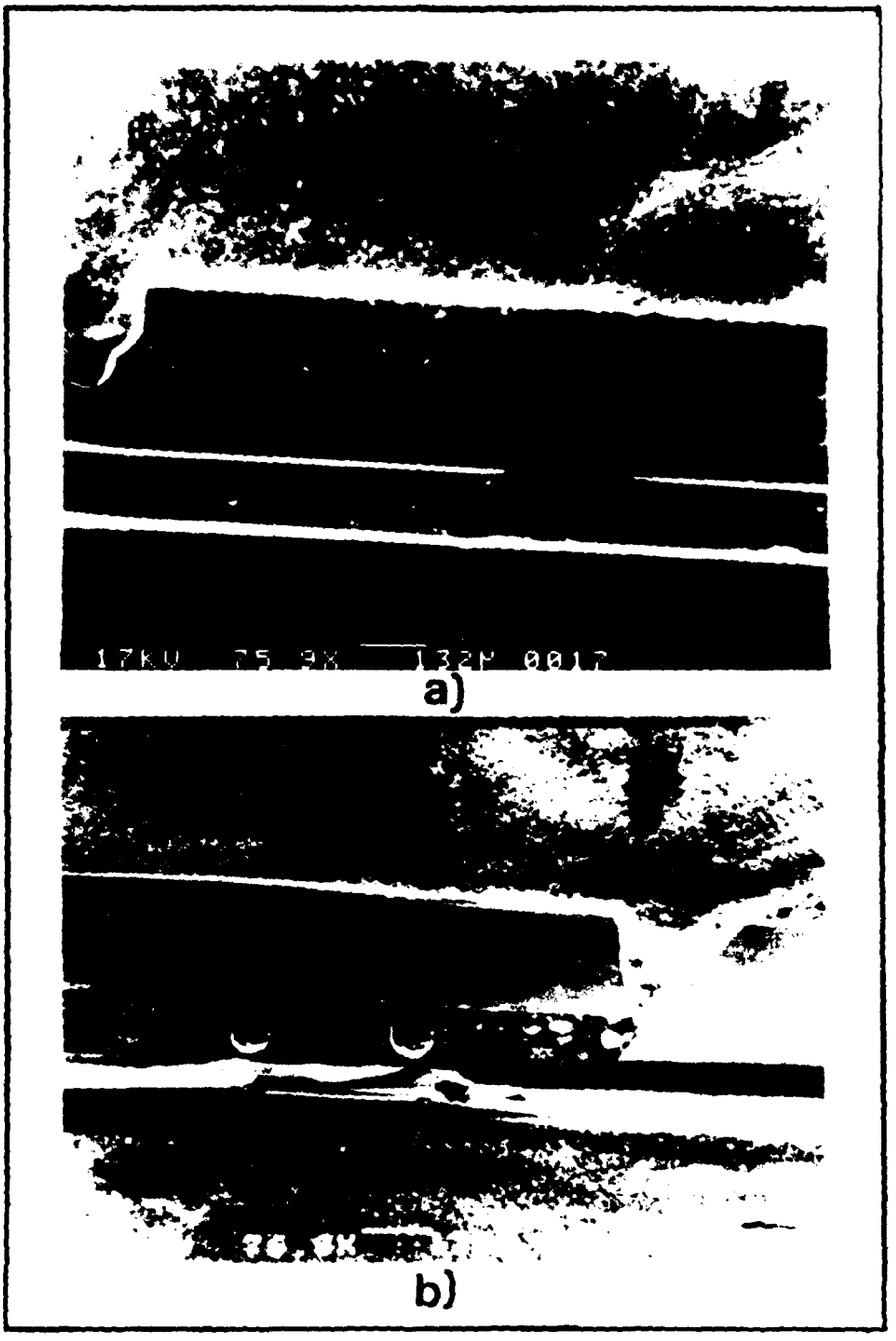


Figure 4-14. Typical Results of Bonding Die in the Wells With the Master Bond EP-34CA Special Epoxy. a) Typical adhesive layer, b) occurrence of small, infrequent voids. The magnification factor of both photographs is 76X.

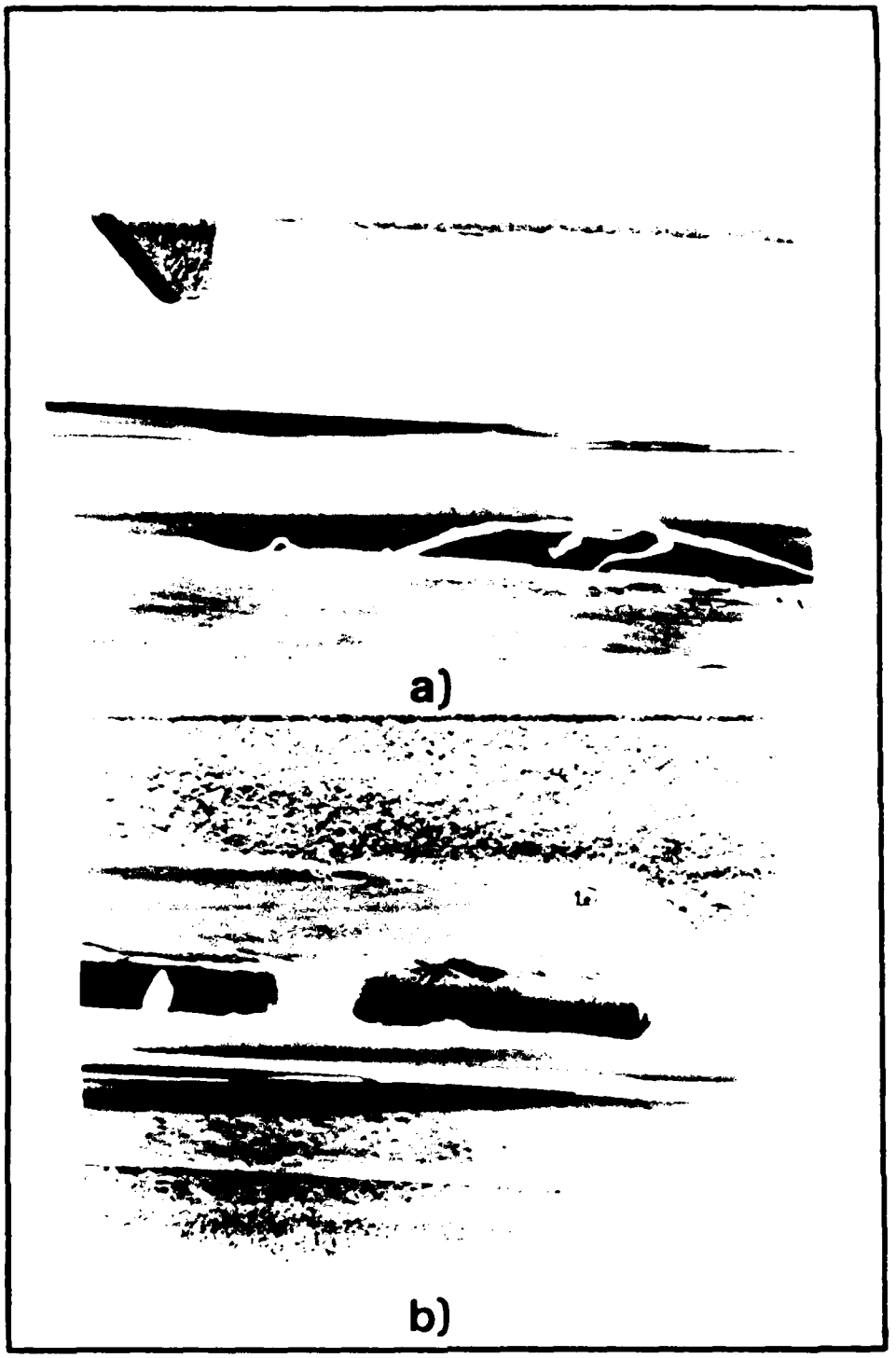


Figure 4-15. Typical Results of Bonding Die in the Wells With the Quantum Materials QMI-2419 Silver Glass Epoxy. a) The adhesive could provide areas of voidless bonding. b) Under the center of the die, large voids formed. The magnification factor on both photographs is 76.8X.

Table 4-III. Summary of the Results of the Die Attach Adhesive Study.

Adhesive	Adhesion Quality		Ease of Application	Highest Process Temp. (o C)	Comments
	Pry Test	SEM Photos revealed			
AuSi	Failed	--	Fair	370	
AuGe	Failed	--	Fair	356	
AuSn	Failed	--	Fair	280	
Dynaloy SM-200	Passed	Severe voiding	Very Good	150	
Amicon ME-990	Passed	Large voids on edges due to shrinkage	Very Good	150	
Master Bond EP34CA Special	Passed	Low to moderate amount of voiding	Good	125	RECOMMENDED
Quantum Materials QMI-2419	Passed	Large areas of voiding	Fair	435	

Key To Comments On "Ease of Application":
Very Good: Optimal ease of application.
Good : Not optimal, but relatively easy; some mixing involved or precise cure temperature needed.
Fair : Inherent difficulties in application or cure; precise cure schedule; special equipment needed.
Poor : Very difficult to apply or cure.

optimum adhesive.

Analysis of the Results. The Master Bond EP-34CA Special two-component epoxy yielded the best results and is recommended for use in the Hybrid Wafer Scale Integration process. Of the seven adhesives tested, it possessed the least voiding problem. It's special characteristic of it being matched to the thermal coefficient of expansion (T.C.E.) of silicon promises to minimize the reliability problems in this silicon-to-silicon bond. EP-34CA Special epoxy is relatively easy to mix and apply, and easy to solvate with acetone. This epoxy is thermally conductive, electrically non-conductive, and provides a strong reliable bond. Another advantage to bonding the die with this epoxy is that the epoxy could also be used for filling the gap region. Excess epoxy from under the die can be allowed to fill the gap. Once cured, additional epoxy can be added to that which is already in the gap and cured. The ability of this epoxy (which is an electrically non-conductive material with a silicon matching T.C.E.) to fill the gap region gives EP-34CA a further advantage compared to the other adhesive candidates.

The gold eutectic materials failed to provide a reliable bond. It is likely that without a scrubbing action and an inert bonding environment, the native oxide forming on the silicon will not be sufficientally disturbed to allow the bond to form (35). Ultrasonic vibration did not have the intended effect on the bonding process which was to provide an alternate technique to achieve a scrubbing action.

The single-component epoxies provided adequate bonding but were plagued with excessive voiding. Possibly, the Dynaloy epoxy outgasses

and the small voids are a result of trapped gas pockets. The Amicon epoxy yielded large void cavities that are attributed to shrinkage during cure.

The silver glass adhesive provided reliable bonding, but occasionally, large voids were present. This fact and its high processing temperature make it a poor choice for the process. The processing temperature (435 degrees Celsius) could cause the electrical characteristics of VLSI die to be changed.

Recommended Adhesive. The Master Bond EP-34CA Special two-component epoxy is recommended for use in the fabrication of final samples. After review of its performance in actual working samples, a recommendation will be made regarding its suitability in the HWSI process. This recommendation will be made in Chapter V.

Fabrication Of Samples For Electrical Testing

The third phase of this research involved the fabrication of samples that demonstrated and validated the goals of the HWSI scheme (Chapter I, Problem Statement). Using the silicon wafer orientation and etchant combination recommended from the WODE study ((100) silicon wafers and Buffered KOH in DIW etchant), and the die attach adhesive recommended in the DAA study (Master Bond EP-34CA Special), test samples were fabricated. Next, the gaps regions were filled with the Master Bond EP-34CA Special epoxy, and the wafers were conformally planerized with the Merck Selectilux HTR 3-200 polyimide. Vias from the top surface of the polyimide layer to the bonding pads on the die were formed before curing the polyimide. After cure, the wafers were coated with a thin film of aluminum which was subsequently patterned into discrete

conductors using standard processing techniques. After annealing the conductors, the samples were ready for evaluation.

Details on the results of the processing steps outlined above are given in the next section. Several minor experiments were carried out to determine the optimal processing materials, techniques, and temperatures. The results of these experiments are also discussed.

Preparation of Die. The procedure used to fabricate mountable integrated circuit die was successful. Six silicon wafers (16 die per wafer) were processed without any failures, resulting in 96 die fabricated with edge dimensions of 197 mils by 197 mils, and a thickness of 8.7 $\pm$ 0.3 mils. A typical die is illustrated in Figure 4-16. A random continuity check of 15 die (3 conductors per die) revealed no conductor failures (such as open conductors) and virtually zero resistance for each conductor.

Etching of (100) Wafers. The results of etching the substrates for the HWSI samples are discussed in the next section.

Etching of Wafers for Final Samples. Twenty-four quartered 3-inch wafers were etched yielding a stock for further processing. The desired well depth was 246 microns (9.7 mils). After etching the wafers for 4 hours and 21 minutes, the etching process was terminated. The well depths were measured with an optical microscope and found to be consistently 244 $\pm$ 1 microns (9.64 $\pm$ 0.04 mils). The etch rate was calculated to be 0.94 microns per minute.

Many of the etched wafers yielded well surfaces that were very smooth and mirror-like, as observed in the WODE study (Figure 4-7). After evaluation (reported in next section), these quality wafers (12 of 24 or 50% were rated quality wafers) were held in storage for later use

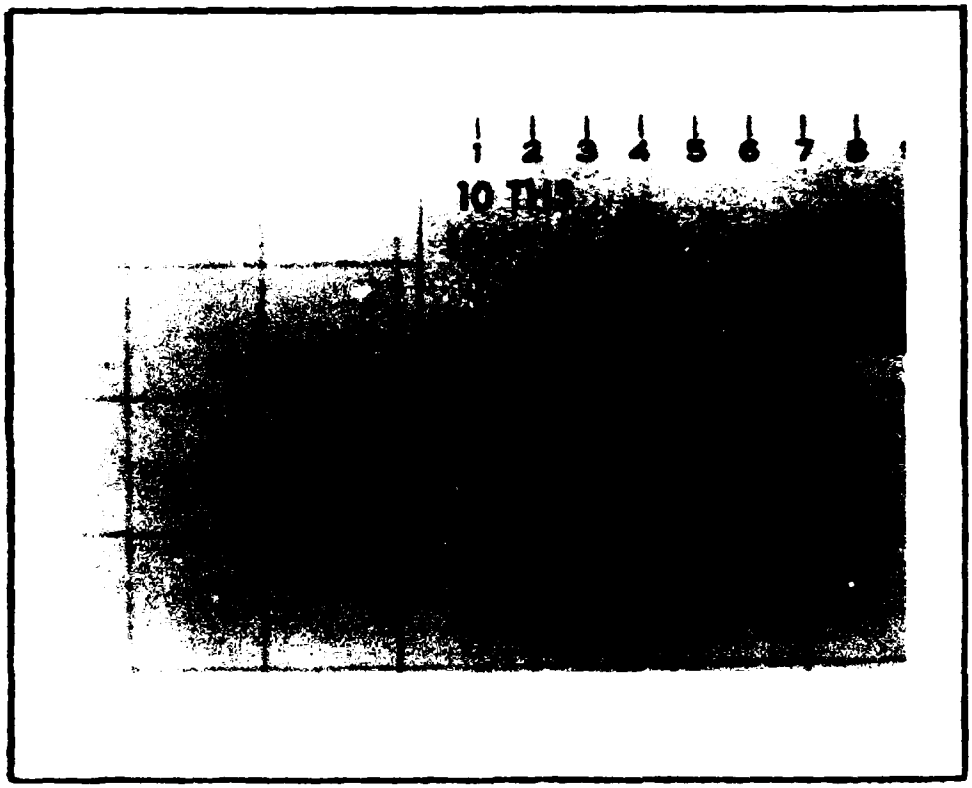


Figure 4-16. Mountable Integrated Circuit Die Used to Prepare the Final Samples. Each die has three aluminum conductors with bonding pads. The die is 197 mils by 197 mils square. The magnification factor is 3X.

in the preparation of the final samples. Other wafers had etching defects, best described as miniature pyramids, on the well's bottom surface with heights of 1-2 mils. These defects are illustrated in Figure 4-17. Many times, the defect only affected one or two of the wells on a wafer. These were classified as slightly defective (7 of 24 or 29%) and stored for use in later processing experiments. The wafers which had multiple pyramid defects on more than three wells were classified as defective (5 of 24 or 21%) and stored with no intention of using them for future work.

Evaluation of the Results. The results of the well's top surface edge length dimensions (made on six randomly chosen quality wafers) are given in Table 4-IV.

The accuracy of the measurements is restricted by the Coordinatograph (reported to be ± 1 mil) The results show that the wafers consistently have internal well dimensions of sufficient size to accommodate the 197 mil square die.

Die Attach Procedure. Using the technique described in Chapter III, a lot of six wafers with six bonded die was fabricated. During several of the earlier attempts to fabricate the test samples, the glass and weight were allowed to remain in position too long (more than 5 minutes). As epoxy filled the gap region and began to cure, it caused the glass and wafer to be bonded together, and thus, the sample was ruined. When bonding the die into the wafer's wells, care must be taken to remove the glass and weight, and periodically clean all surfaces with acetone (2 to 5 minute intervals) until epoxy no longer appears on the glass surface. One of the prepared wafers is illustrated in Figure 4-18.

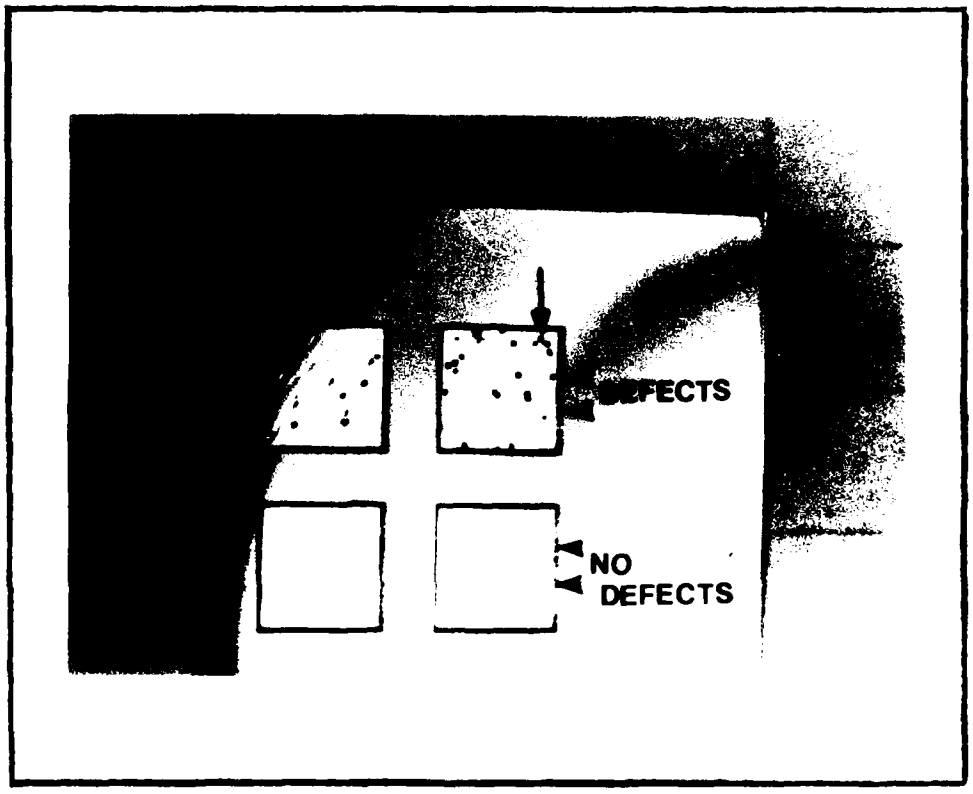


Figure 4-17. Pyramid Defects Which Occur When Etching (100) Silicon. The etchant was a mixture of potassium hydroxide, deionized water, and isopropyl alcohol heated to 80 degrees Celsius. The arrow indicates a cluster of defects. Note that these defects occur in some wells, but not in adjacent wells. The magnification factor is 3X.

Table 4-IV. Evaluation of the Well Bottom's Edge Length.

Wafer Number	WELL NUMBER					
	1	2	3	4	5	6
1	202/201	203/202	202/202	202/202	203/202	201/202
2	201/201	201/202	202/202	202/201	201/202	202/202
3	202/202	202/203	202/201	200/201	202/201	201/202
4	203/203	204/203	203/204	203/203	203/204	203/204
5	200/201	201/201	201/201	201/200	201/202	201/201
6	201/202	202/201	202/201	202/201	202/201	201/202

Measurements in mils.
The estimated accuracy of the measurements is + 1 mil.

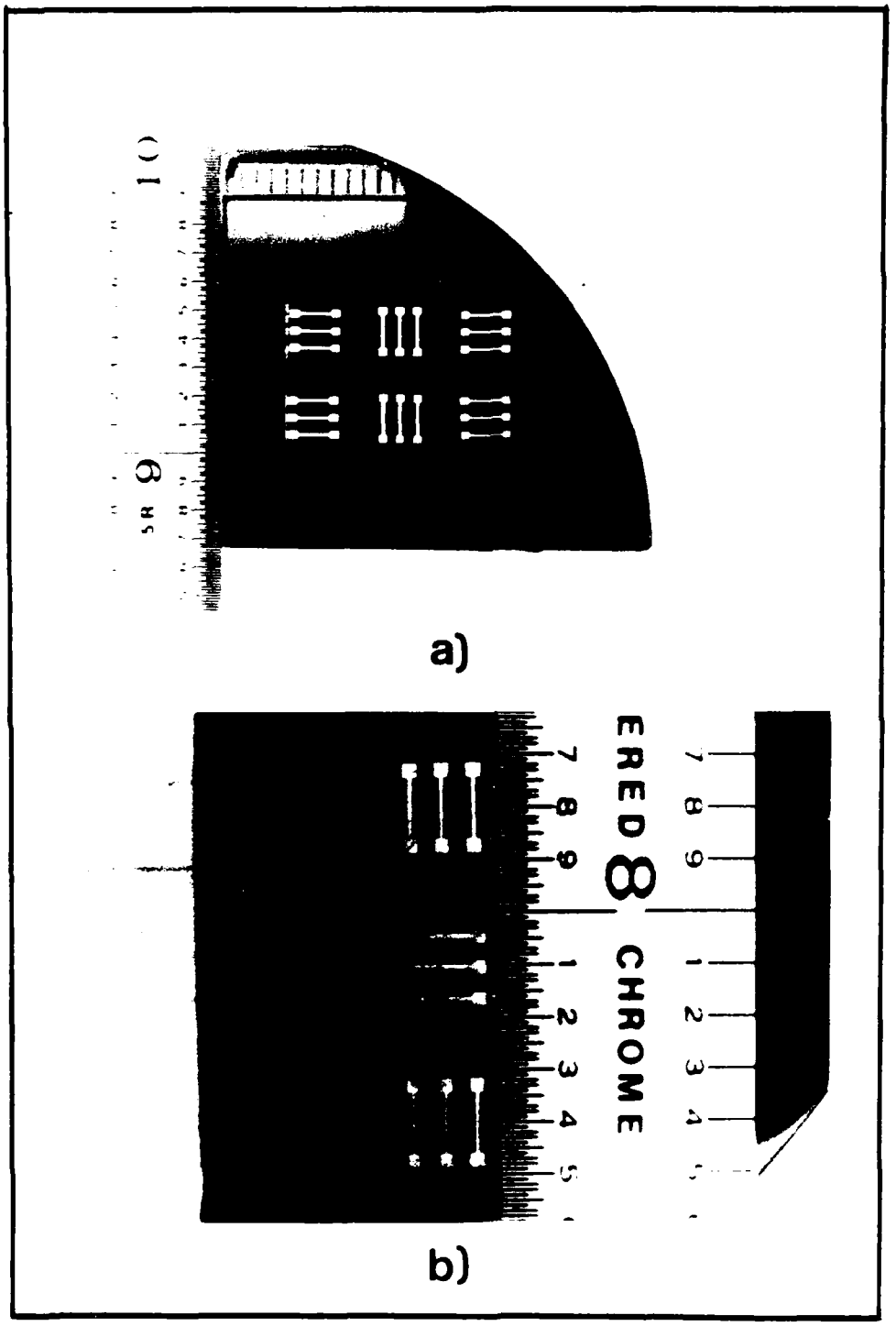


Figure 4-18. A Typical Sample Before Application of Polyimide. a) Full view; the magnification factor is 1.8X and b) Closeup view; the magnification factor is 3.0X.

Evaluation of the Master Bond EP-34CA Special Epoxy as a Gap Filler. The procedure to fill the gap with the Master Bond EP-34CA Special epoxy was found to be adequate to fill at least 75% of the gap's volume. Figure 4-19 illustrates a typical amount of fill rendered by this procedure after it was accomplished twice. Due to epoxy shrinkage, a meniscus formed at the top surface of the epoxy. The photographs in Figure 4-19 also reveal voiding in gap's volume. Finally, the cross-sectional photographs reveal that the gap filling procedure is moderately successful in providing a smooth surface upon which the polyimide can be applied.

Effect of Processing Temperature on Further Process Steps. The purpose of this experiment is to observe the effects of heat on the adhesive layer. The samples were tested at temperatures above the recommended 125 degrees Celsius cure temperature in three steps. The samples, designated A and B (chosen at random from the lot of wafer-die assemblies), were used in this experiment. The procedure implemented was described in Chapter III in the sub-section "Effect of Processing Temperature on Further Process Steps". Table 4-V summarizes the results of the first and second experiments.

The results of the initial experiment indicates that the die shifts or rises out of its original position when subjected to a 350 degree Celsius environment, even when the glass and weight are pressing down on the die. The shifts are relatively large (from 50 to 170 microns, or 2 to 7 mils), and they are unacceptable for this project. It was concluded that the highest tolerable processing temperature spanned 125-350 degrees Celsius. Also noted, is the fact that for each die, a 30 to 50 micron delta measurement already existed. This further indicates that

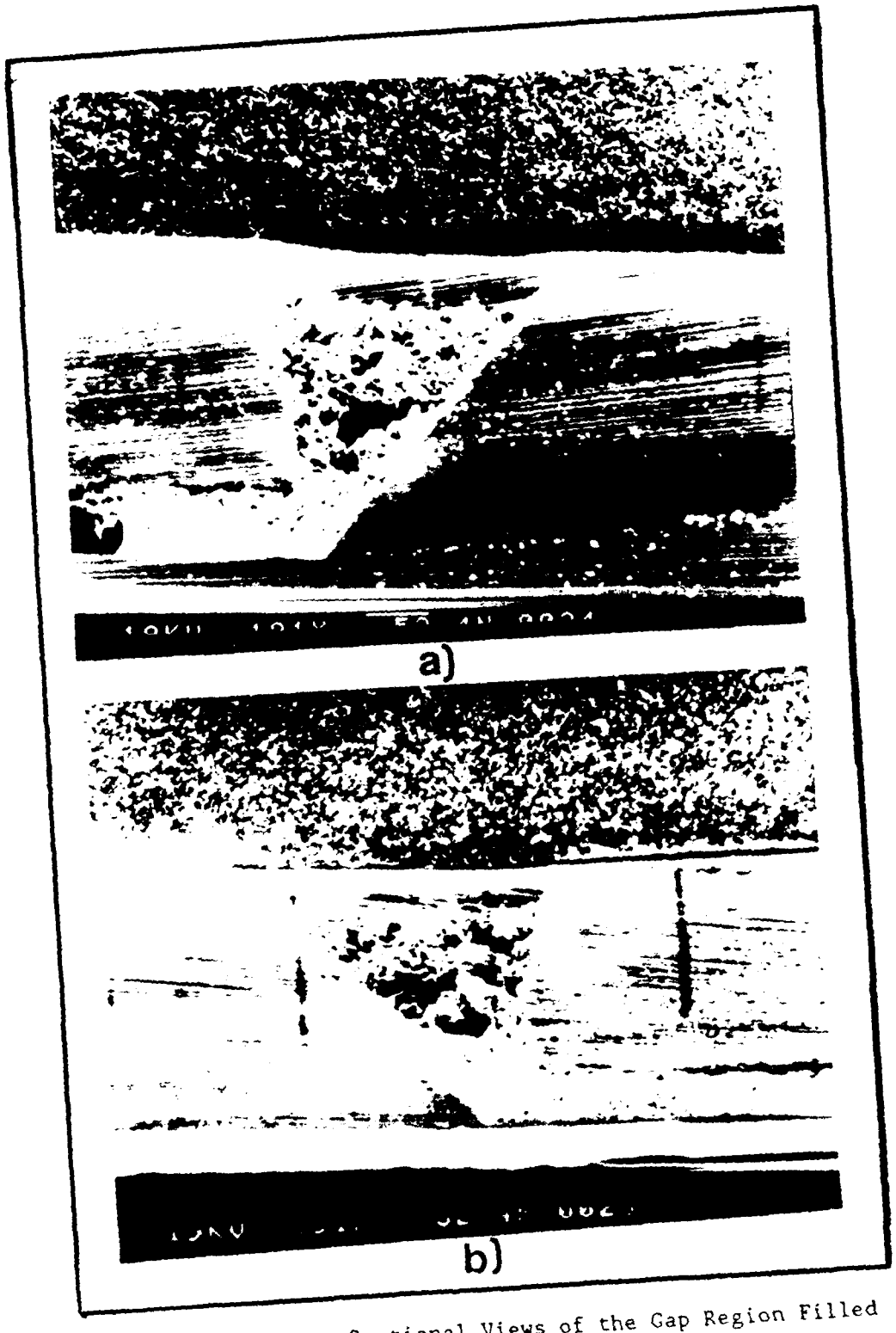


Figure 4-19. Cross-Sectional Views of the Gap Region Filled With the Master Bond EP-34CA Special Epoxy. In both photographs, some voiding is noted in the gap region filled with epoxy. The magnification factor in both photographs is 191X.

Table 4-V. Effect of Processing Temperature on Sample A.

Temperature Cycle	Location on Wafer (see Figure 3-10)											
	1	2	3	4	5	6	7	8	9	10	11	12
Initial	30	40	40	30	40	30	50	40	30	40	40	50
After 1st 350 degrees test	110	110	90	130	90	100	140	210	105	100	110	110
After 2nd 350 degrees test	100	130	90	130	90	100	140	205	100	100	110	120
All measurements in microns and rounded to the nearest 5th micron.												

even with the glass and weight in place, sufficient pressure accumulates under the die to cause it to rise slightly while curing. The 350 degree Celsius temperature seems to aggravate the problem.

In the second experiment, the test samples were exposed to the 350 degree Celsius environment without the cover glass and weight. The significant result of this experiment was that the die did not shift further out of the positions they were in at the end of the first test.

In the third experiment, another sample (B) was placed in an oven whose temperature was 150 degrees Celsius. The temperature was increased in steps of 25 degrees Celsius, up to 350 degrees Celsius. The sample remained at each temperature for 30 minutes, and then was removed from the oven and allowed to cool. Then, the delta measurements were taken using the optical microscope. The results of this experiment are given in Table 4-VI and Figure 4-20. These results show that at temperatures between 125 degrees and 200 degrees Celsius, the adhesive layer actually shrinks. This fact was discovered by averaging the measurements taken of the delta measurements at a specific temperature. Above 200 degrees, the die began to rise in relation to their original position after cure. Between 200 and 350 degrees Celsius, the die rose an average of 70 microns above their original positions. Arbitrarily, the criteria for setting the maximum processing temperature was determined to be the temperature at which the die shifted by no more than 10% of this amount or 7 microns (that is, the temperature is approximately 250 degrees Celsius). Consequently, the maximum processing temperature was chosen to be 250 degrees Celsius.

Table 4-VI. Effect of Processing Temperature - Sample B.

	WELL NUMBER												Average Change Compared To Initial Values in microns
	1		2		3		4		5		6		
	1	2	3	4	5	6	7	8	9	10	11	12	
Initial	40	50	30	40	40	20	40	50	30	40	60	40	0.0
After 150 degrees	30	40	30	40	40	30	40	50	35	40	60	40	- 0.4
After 175 degrees	35	40	30	40	30	30	40	50	35	40	60	40	- 0.8
After 200 degrees	35	40	30	40	30	30	40	50	35	40	60	40	- 0.8
After 225 degrees	35	40	35	40	35	35	40	50	35	40	55	50	+ 0.8
After 250 degrees	35	45	40	45	55	50	35	55	35	45	45	55	+ 4.0
After 275 degrees	45	55	50	55	65	60	55	70	45	55	60	70	+ 16.3
After 300 degrees	70	75	75	75	75	70	85	95	65	65	75	80	+ 43.8
After 325 degrees	90	95	90	85	85	85	105	125	85	85	105	95	+ 64.2
After 350 degrees	110	110	105	100	90	100	140	170	105	100	130	100	+ 90.0

All temperatures are in degrees Celsius. All measurements in microns. The "average change" values in the right column were calculated by averaging each row and subtracting the value of the initial average.

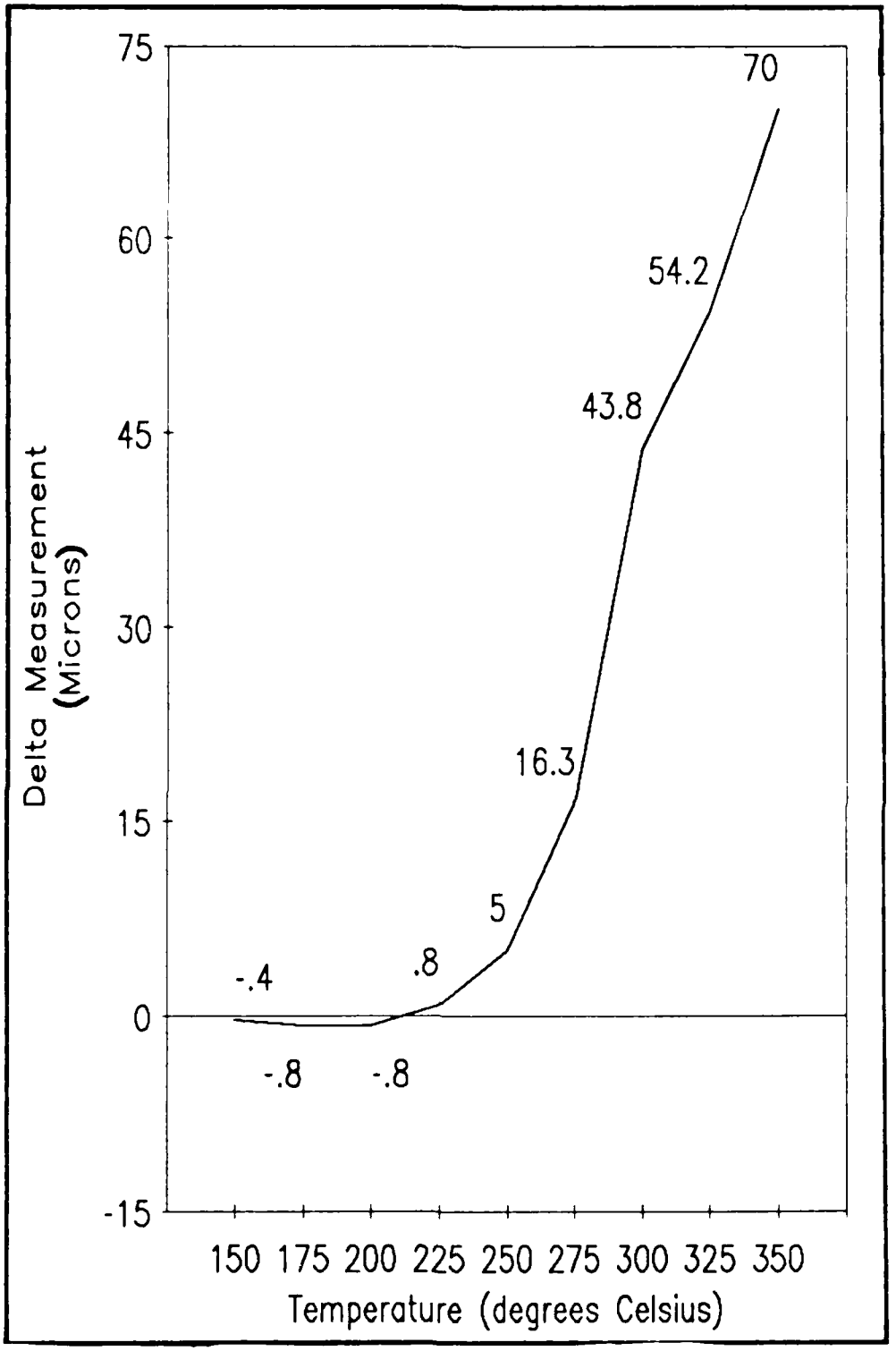


Figure 4-20. Results of the Test to Determine the Effect of the Processing Temperature on the Shift of a Die in It's Well. The graph shows that above 250 degrees Celsius, the die shifts (rises) in the well by 7 microns (10% of total 70 micron shift).

Application of Photosensitive Polyimide as a Planarizing Inter-Metal Insulator. The photosensitive polyimide was easy to apply, and it yielded excellent results for planarizing the surface of the HWSI test samples.

Via Fabrication Experiment. The via fabrication experiment sought to determine the optimal proximity printing distance to realize sloping side walls. The processing of the wafers for the via fabrication experiment was successful, and the results are presented in Table 4-VII.

The results of this experiment show that the optimal proximity distance is 27 mils. Micrographs of one of the vias resulting from each proximity distance evaluated are presented in Figures 4-21 and 4-22. The results demonstrate that annealing after evaporation and patterning, yields a more reliable electrical contact at the vias. Therefore, annealing at 250 degrees Celsius is recommended.

Application of the Polyimide. The polyimide was applied to six final samples. The thickness after cure for all of the samples was approximately 10 microns. The cure temperature was limited to 250 degrees Celsius. It is recognized that this fact could potentially cause reliability problems. Figure 4-23 depicts a chart which shows the degree of imidization of the polyimide versus the cure temperature (30:6). The chart shows that for a 250 degree Celsius cure, an 83-85% imidization occurs. This degree of imidization seems to achieved at the temperatures of 200 to 350 degrees Celsius. The choice of a 250 degree Celsius cure temperature (rather than a lower 200 to 225 degree Celsius cure temperature) assures that at least this degree of imidization takes place. Incomplete imidization leaves moisture in the layer which may cause long-term reliability problems. The effect of higher temperatures on the

Table 4-VII. Results of the Via Fabrication Experiment.

Proximity Distance	Number of Vias Which Conducted	Percentage of Conducting Vias
0 mils (before anneal)	14 of 36	38.9%
0 mils (after anneal)	21 of 36	58.3%
13.5 mils (before anneal)	22 of 35	62.8%
13.5 mils (after anneal)	24 of 35	68.6%
27.0 mils (before anneal)	25 of 36	69.4%
27.0 mils (after anneal)	30 of 36	83.3%
40.5 mils (before anneal)	21 of 32	65.6%
40.5 mils (after anneal)	26 of 32	81.2%

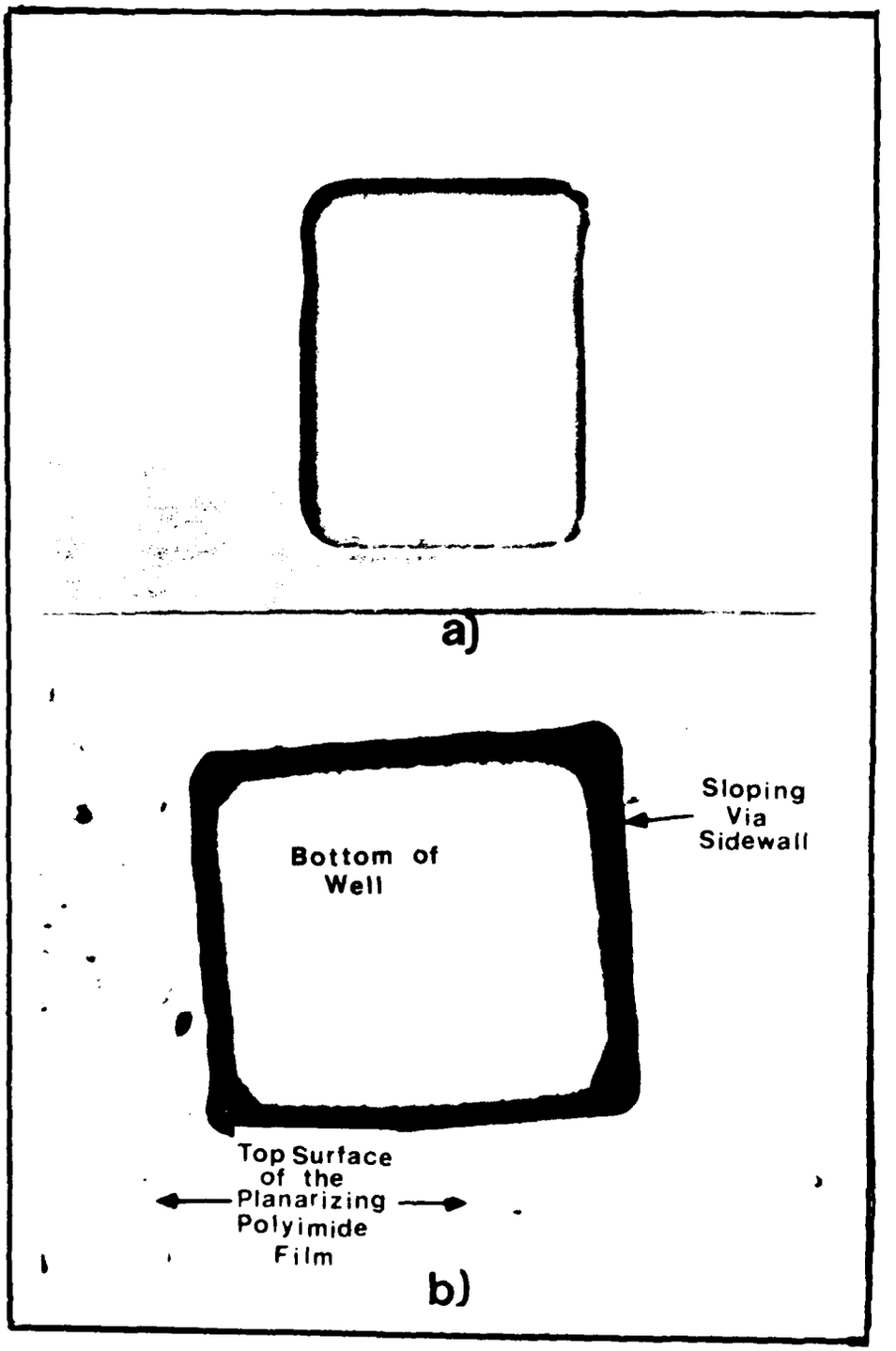


Figure 4-21. Micrograph of a Via Exposed With Contact Printing (a) and a Proximity Distance of 13.5 mils (b). The magnification factor for both photographs is 375X.

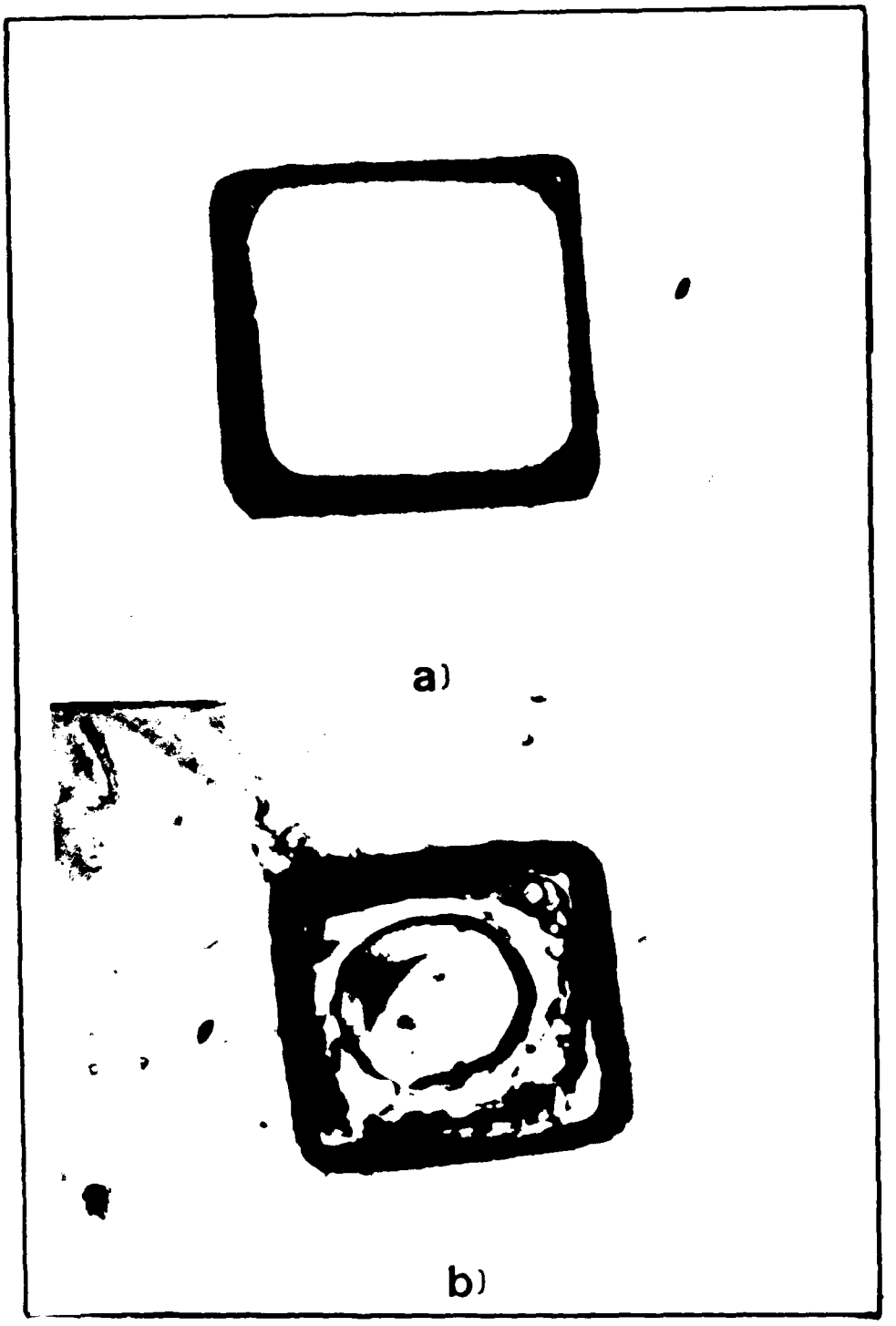


Figure 4-22. Micrograph of a Via Exposed With a Proximity Distance of 27.0 mils (a) and 40.5 mils (b). The magnification factor of both photographs is 375X.

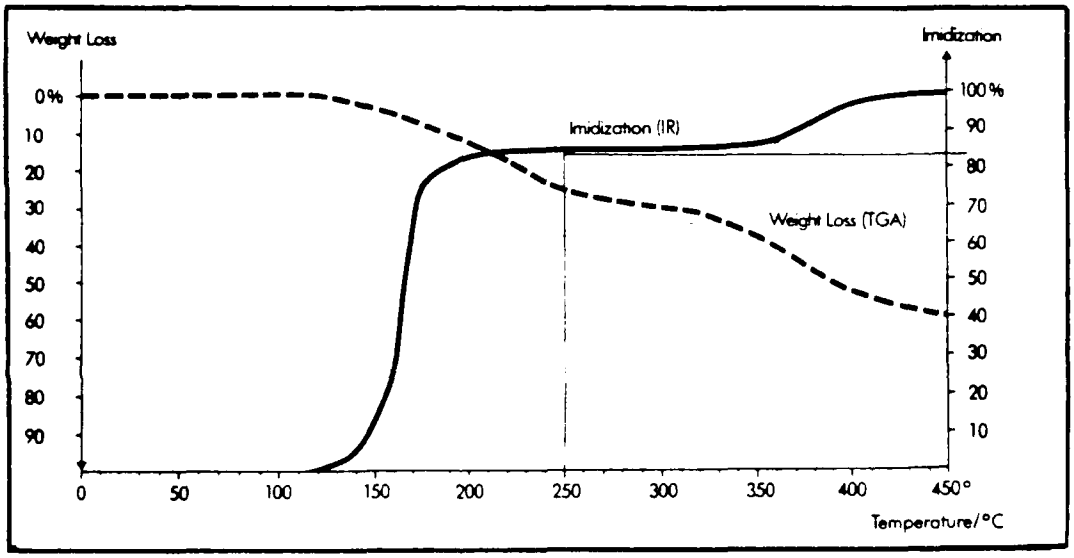


Figure 4-23. Degree of Imidization Versus Cure Temperature. A 250 degree Celsius cure temperature yields 83-85% imidization (30:3).

samples was investigated in the evaluation phase of this research project. Figure 4-24 shows cross-sectional SEM photographs of the gap regions of the test samples coated with Selectilux HTR 3-200. The top photograph shows a sample with a very small delta measurement, and the bottom photograph shows a sample with a larger delta measurement. For both situations, the degree of planarization is adequate to provide a smooth surface for metal conductors to transition from the support substrate to the die.

Metallization of Samples. Following the deposition of the polyimide layers on the six final samples, the focus turned to evaporating a thin film of aluminum on each sample and patterning the film into discrete conductors. The standard process of evaporating aluminum is presented in Appendix G. Before the final samples were metallized and patterned, the photoresist and aluminum anneal experiment was accomplished, and the results are given below.

Photoresist and Aluminum Anneal Experiment. This experiment was carried out to determine whether annealing had an appreciable effect on the conductivity of the aluminum thin films. The via fabrication experiment clearly demonstrated the advantage of annealing for improving via conductivity. This experiment also had the goal of determining the superior photoresist (positive or negative) for this process.

After the metal was evaporated onto the samples, the sheet resistance of each sample was measured. Samples A and C were then annealed at 350 degrees Celsius, cooled, and the sheet resistance measurement was re-accomplished. The sheet resistance measurements are presented in Table 4-VIII.

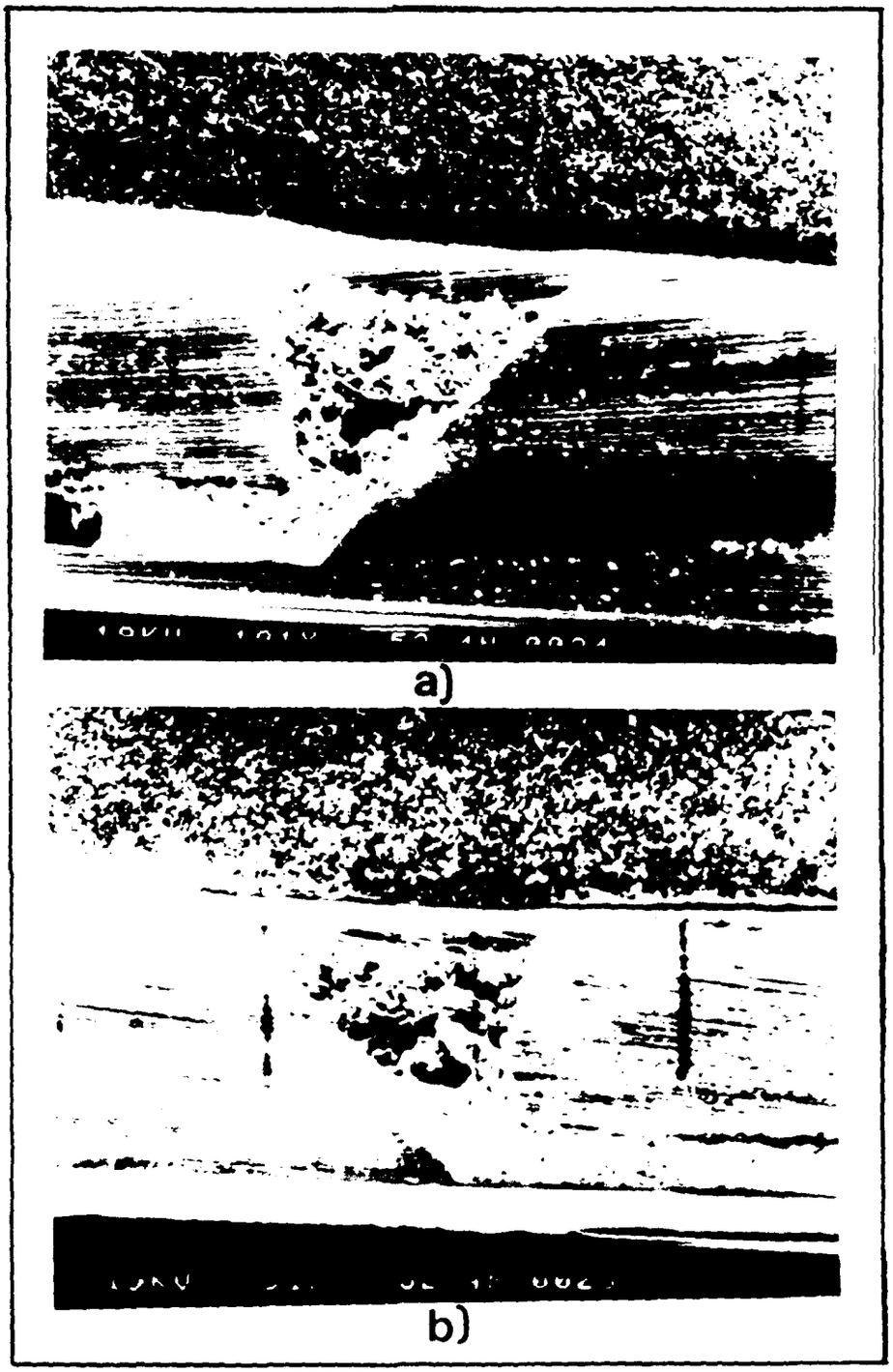


Figure 4-24 Cross-Sectional SEM Micrographs of the Gap Regions of Samples Coated With Polyimide. The polyimide layers are approximately 10 microns thick on both samples. a) The gap transition has a small delta separation of 10 microns. b) The gap transition has a delta separation of 40 microns. The magnification factor of both photographs is 191X.

Table 4-VIII. Sheet Resistance Measurements of Annealed Versus Non-Annealed Samples.

Sample	Sheet Resistance (Ohm/square)	Standard Deviation
Preannealed:		
A	0.00183	5.99%
B	0.00181	4.79%
C	0.00173	2.26%
D	0.00172	1.60%
Postannealed:		
A	0.00180	5.34%
C	0.00172	1.26%
Standard deviation calculations were made by the instrument.		

There was essentially no change in the sheet resistance as a result of annealing the aluminum. The changes were on the order of one part in 100,000.

The samples were coated with the photoresists (positive resist for samples A and B; negative resist for samples C and D), exposed, and the aluminum was etched. The etching time was 10 minutes. The resulting metal patterns were examined visually, and a continuity check was performed on the conductors. All of the conductors on all four samples had a resistance value of 0.5 $\pm$ 0.1 ohms. Samples A and B (positive photoresist) had defect-free, sharply-patterned conductors. In contrast, samples C and D had conductors with rough, ill-defined edges. It was clear that the positive resist held the greatest promise for use in the photolithography steps of the metallization and etch process.

Metallization of the Final Samples. Using the results of the photoresist and aluminum anneal experiment described in the prior section (results reported in Chapter IV), the final test samples were metallized and etched to delineate the metal conductors. The test samples were metallized using the thermal evaporation technique; this procedure is described in Appendix G. Six test samples were metallized in two groups of three. The first group of three had an aluminum thickness of 2.2 microns. The second group had an aluminum thickness of 2.1 microns. Following the aluminum evaporation, the samples were annealed at 250 degrees Celsius for 30 minutes.

Patterning the Final Samples. Following the anneal process, the thin film of aluminum was patterned to define discrete conductors. To achieve this step, the aluminum that was to remain as the conducting path needed to be protected from the etchant. This requirement was

satisfied by spinning positive photoresist onto the surface of the aluminum, prebaking it, and exposing it to ultraviolet light with an appropriate photomask that shielded the areas to be stripped of metal. A difficulty arises if the photoresist fails to adequately protect the metal conductors where the metal passes over the transition region between the support substrate and the die. The etchant will remove the metal from these unprotected areas and open circuits or breaks will result. Single and multiple photoresist layers were checked for adequacy in protecting the metal conductors. The results of this investigation are given below.

Single Photoresist Layer. The results for using a single coat of positive photoresist to protect the conductors during etch revealed that it was not adequate protection at the gap regions. Any sharp-edged discontinuity in the topography of the polyimide layer caused the photoresist at that point to be very thin. This problem was observed to be greater at the gap regions where the deltas are large (greater than 50 microns).

Multiple Photoresist Layers. A three layer application of positive photoresist provided adequate coverage at the gap regions. Therefore, the application of a triple coat of photoresist is recommended for the HWSI fabrication process, and was utilized to prepare the final test samples.

Etching of the Aluminum. After the final samples were coated with a triple coat of positive photoresist and postbaked, they were etched in a fine-resolution etchant (Appendix D) for approximately 10 minutes. The six samples were etched in two groups of three. In the

first etching attempt, one group was accidentally overetched, and the samples were lost. The second group (metal thickness of 2.1 microns) was successfully etched. No additional etching problems were encountered.

Removal of the Photoresist. Losolin was used to remove the triple coat of photoresist from the remaining three samples. It was found to quickly and safely remove the resist without altering the underlying polyimide or aluminum.

Evaluation of the Final Samples.

Three final test samples (referenced as A, B, and C) were successfully prepared using the procedures described in the previous section. In order to determine the effectiveness of the entire fabrication process, these samples were subjected to several electrical and thermal tests. The results of these tests are described in the next section.

Continuity Test. The results of the continuity test are presented in Table 4-IX.

Mean-Time-To-Failure Tests. Two mean-time-to-failure tests were performed: one at room temperature (20 degrees Celsius) and the other at 150 degrees Celsius. Both lasted for 60 hours duration. A 1 kHz unipolar square wave with a peak current of approximately 50 milli-amperes was passed through each circuit. The room temperature test produced three failures. Since there were 16 early failures observed in the results of the continuity tests, the three failures represent 3 of 39 or a 8.7 failure percentage. The results of this test are summarized in histogram form in Figure 4-25. The 150 degree Celsius test also resulted in three failures. Since 19 circuits had failed prior to this test, the

Table 4-IX. Initial Resistance Values of Each Circuit.

		SAMPLE		
DIE	CIRCUIT	A	B	C
	1	1.4	---	8.9
1	2	---	2.6	9.2
	3	1.5	2.8	10.1
	4	1.6	---	---
2	5	0.8	2.8	---
	6	0.9	4.8	---
	7	1.1	---	---
3	8	0.8	---	1.3
	9	16.0	---	---
	10	0.8	5.7	2.3
4	11	---	2.9	---
	12	1.1	2.0	3.1
	13	0.8	1.6	6.9
5	14	1.5	---	3.3
	15	---	---	6.6
	16	8.6	1.1	4.2
6	17	0.9	2.5	2.2
	18	2.0	0.8	7.9

The readings are in ohms; an open circuit is indicated by ---.

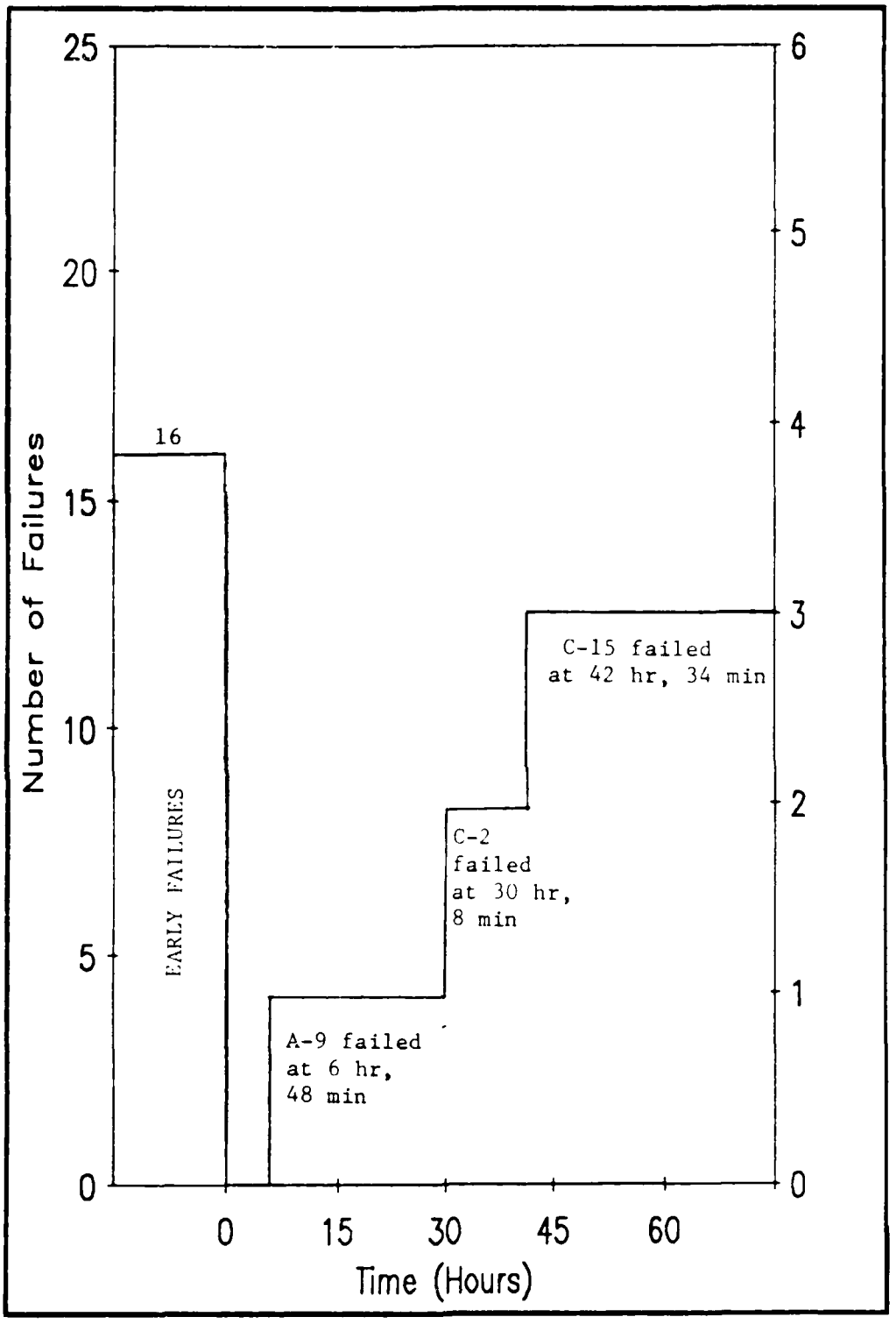


Figure 4-25. Histogram Showing Results of the Room Temperature Mean Time to Failure Test. Sixteen early failures had occurred before the test. Three failures occurred during the test. The time of failure is indicated.

three failures represent 3 of 35 or an 8.6 percent failure rate. The results of this test are illustrated in Figure 4-26.

High Temperature Tests. These tests sought to determine the effect of high temperature on the polyimide, and thus, the resulting effect on the conductivity of the conductors across the substrate-to-die transition and in the vias. The results of these tests are discussed below.

Rapid Temperature Increase Test. The purpose of this test was to observe the results of subjecting one sample to a rapid temperature increase. Sample C was placed on a hotplate calibrated to 350 degrees Celsius. Within 30 seconds of placing the sample on the hot plate, the polyimide layer began to bubble severely. Large areas of the polyimide coating (along with the aluminum conductors) separated from the surface of the sample. A photograph of this sample is shown in Figure 4-27.

Ramped Temperature Test. The purpose of this test was to observe the results of gradually heating a sample to 350 degrees. Sample A was placed in a forced air oven set at 175 degrees Celsius for 30 minutes, removed, and inspected. The sample was then returned to the oven which had its temperature increased by 25 degrees Celsius. The sample remained at this elevated temperature for 30 minutes, was removed, and inspected. This routine was repeated until the oven temperature reached the 350 degrees Celsius level. The results of the test are presented in histogram format in Figure 4-28. Three additional failures occurred during this test (one at 275 degrees Celsius and 2 at 325 degrees Celsius).

High Temperature Endurance Test. The purpose of this test was to determine the results of leaving the slowly heated sample (sample A from the last test) at 350 degrees Celsius for a period longer than 30

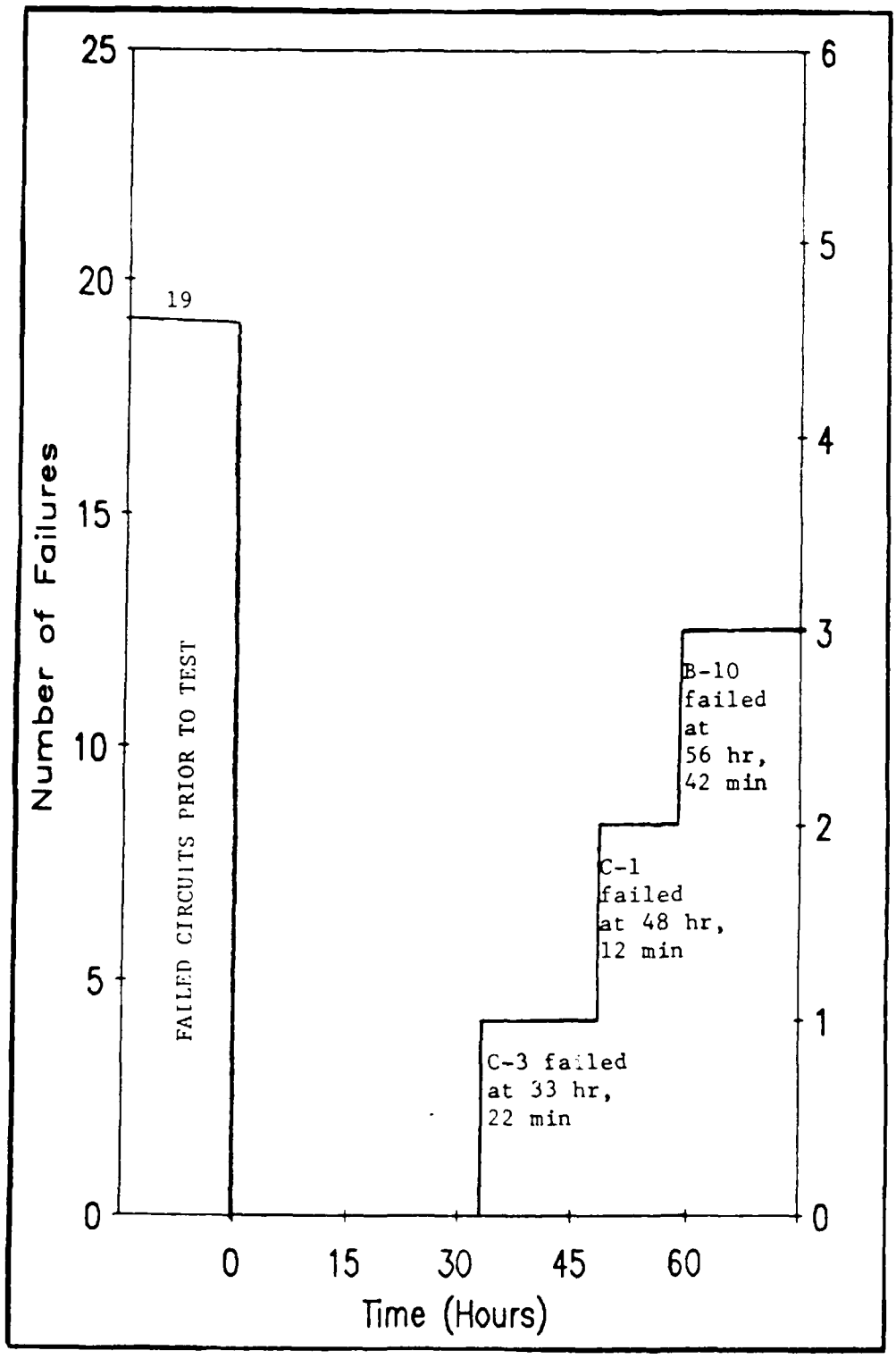


Figure 4-26. Histogram Showing Results of the 150 Degree Celsius Mean Time to Failure Test. Nineteen failures had occurred before the test. Three failures occurred during the test. The time of each failure is indicated.

Figure 4-27. Photograph of Sample "C" After the High Rate of Temperature Increase Test. Within 30 seconds, the polyimide coating had bubbled severely. The magnification factor is 2X.

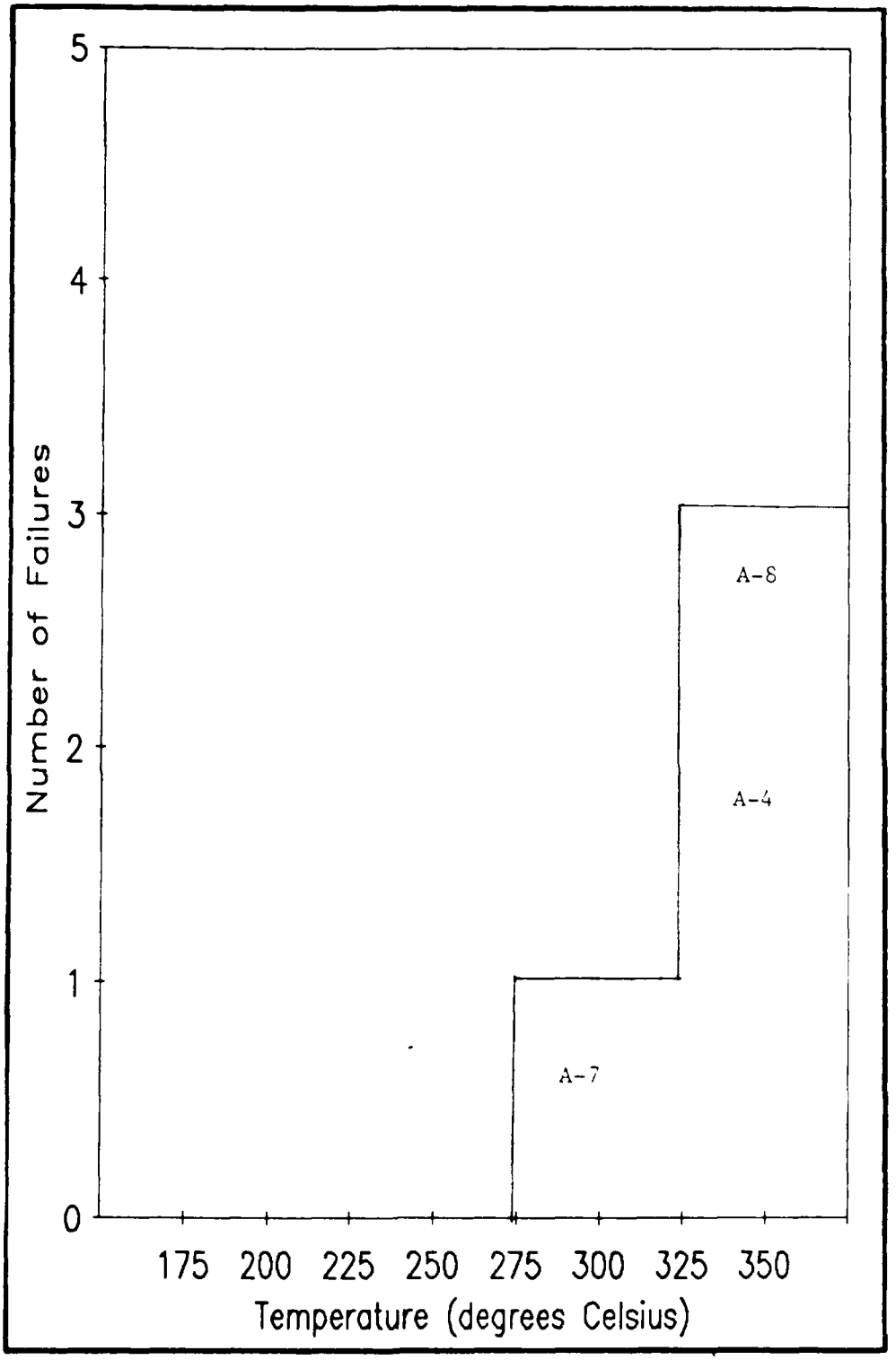


Figure 4-28. Histogram Showing the Results of the Ramped Temperature Test. Three failures occurred during the test. The temperature at which each failure occurred is indicated.

minutes. After sample A had reached the 350 degree Celsius level during the previous test, it was left at that temperature for 16 hours. The sample was periodically removed from the oven at 1, 2, 4, 6, 8, and 16 hours duration, and its condition was observed. No further failures occurred during the prolonged exposure to the 350 degree Celsius temperature. A photograph of sample A after this test is presented in Figure 4-29.

Fault Analysis of The Final Samples. To evaluate the effectiveness of the process, it was important to understand how the samples failed, and how often any particular failure mode occurred. The results of the failure analysis are given in the next section.

Possible Faults. There are two key areas where most circuit failures could occur:

1. At the "gap" region where the aluminum conductors make a transition from the surface of the support substrate to the surface of the mounted die, and

2. Breaks in the conductor occur at the vias. At the transition region, breaks in the aluminum conductor resulted in an open circuit. Likewise, vias may not conduct due to steep sloping sidewalls and insufficient conductor coverage.

Statistical Analysis of Fault Occurrence. Each failed circuit on the three final samples was probed to determine the exact location of the fault causing the circuit to failure. The results of this test are given in Table 4-X where each circuit is listed along with the cause of failure (if appropriate). Table 4-XI is a statistical breakdown of the results of the evaluation of the final samples. Tables 4-XII and 4-XIII

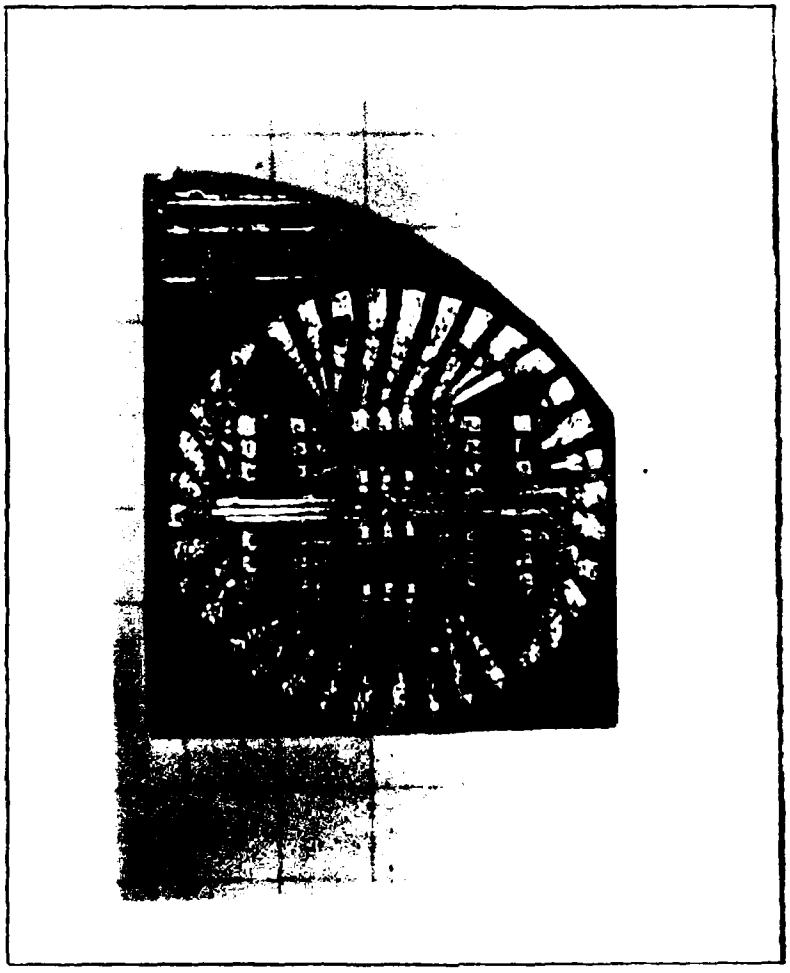


Figure 4-29. Photograph of Sample "A" After The High Temperature Tests. The magnification factor is 2X.

Table 4-X. Results of the Fault Analysis.

DIE	CIRCUIT	SAMPLE		
		A	B	C
1	1	Passed	Via (b)	Gap (a)
	2	Gap (b)	Passed	Gap (a)
	3	Passed	Passed	Gap (a)
2	4	Gap (a)	Via (both)	Gap (a)
	5	Passed	Passed	Gap (a),Via (b)
	6	Passed	Passed	Gap (a)
3	7	Gap (a)	Via (both)	Gap (a)
	8	Gap (both)	Via (both)	Passed
	9	Gap (b)	Via (both)	Gap (both)
4	10	Passed	Gap (a)	Passed
	11	Gap (b)	Accidental	Gap (a)
	12	Passed	Accidental	Passed
5	13	Passed	Passed	Passed
	14	Passed	Via (a)	Gap (b)
	15	Gap (a)	Via (a)	Gap (a)
6	16	Passed	Passed	Passed
	17	Passed	Passed	Passed
	18	Passed	Passed	Gap (a)

KEY

Passed: Circuit survived all tests.
Gap ( ): Failure occurred at the gap indicated in the parenthesis.
Via ( ): Failure occurred at the via indicated in parenthesis.
Accidental: Failure occurred due to accidental loss.
The letter "a" in parenthesis indicates the first gap or via encountered in the circuit; the letter "b" indicates the second gap or via.

Table 4-XI. Statistical Analysis of the Three Test Samples.

Failure Category	SAMPLE			TOTALS
	A	B	C	
Early Failures	3 of 18	7 of 18	6 of 18	16 of 54
Percent of Early Failures	16.7%	38.9%	33.3%	29.6%
Failures - Accidental Loss	0 of 15	2 of 11	0 of 12	2 of 38
Percentage Failed-Accidents	0.0%	11.1%	0.0%	5.3%
Failures - 20 Degree Test	1 of 15	0 of 9	2 of 12	3 of 36
Percent Failed:				
(in relation to remainder)	6.7%	0.0%	16.7%	8.3%
(in relation-original total)	5.6%	0.0%	11.1%	5.6%
Failures - 150 Degree Test	0 of 14	1 of 9	2 of 10	3 of 33
Percent Failed:				
(in relation to remainder)	0.0%	11.1%	20.0%	9.1%
(in relation-original total)	0.0%	5.6%	11.1%	5.6%
Failures - 350 Degree Test	3 of 14	N.A.	2 of 8	5 of 22
Percent Failed:				
(in relation to remainder)	21.4%	N.A.	25.0%	22.7%
(in relation-original total)	16.7%	N.A.	11.1%	9.3%
Survived All Tests	11 of 18	8 of 18	6 of 18	25 of 54
Percent Surviving All Tests				
(in relation-original total)	61.0%	44.4%	33.3%	46.3%

Table 4-XII. Early Failure Analysis.

Failure Category	SAMPLE			TOTALS
	A	B	C	
Early Failures	3 of 18	7 of 18	6 of 18	16 of 54
Percent of Early Failures	16.7%	38.9%	33.3%	29.6%
Failure due to cracks in metallization on one gap	3 of 3	0 of 7	5 of 6	8 of 16
Percentage	100%	0.0%	83.3%	50.0%
Failure due to cracks in metallization on both gaps	0 of 3	0 of 7	1 of 6	1 of 16
Percentage	0.0%	0.0%	16.7%	6.3%
Failure due to no conduction at one via	0 of 3	2 of 7	0 of 6	2 of 16
Percentage	0.0%	28.6%	0.0%	12.5%
Failure due to no conduction at both vias	0 of 3	4 of 7	0 of 6	4 of 16
Percentage	0.0%	57.2%	0.0%	25.0%
Failure due to breaks in both a gap and a via	0 of 3	1 of 7	0 of 6	1 of 16
Percentage	100%	0.0%	83.3%	6.3%

Table 4-XIII. Analysis of Failures Occurring During Tests.

Failure Category	SAMPLE			TOTALS
	A	B	C	
Failures During Test Percent of Early Failures	4 of 15 26.7%	3 of 11 27.3%	6 of 12 50.0%	13 of 38 34.2%
Failure due to cracks in metallization on one gap Percentage	2 of 4 50%	0 of 3 0.0%	6 of 6 100%	9 of 13 69.2%
Failure due to cracks in metallization on both gaps Percentage	2 of 4 50%	0 of 3 0.0%	0 of 6 0.0%	2 of 13 15.4%
Failure due to no conduction at one via Percentage	0 of 4 0.0%	0 of 3 0.0%	0 of 6 0.0%	0 of 16 0.0%
Failure due to no conduction at both vias Percentage	0 of 4 0.0%	0 of 3 0.0%	0 of 6 0.0%	0 of 16 0.0%

are analyses of the early failures and the failures which occurred during the mean-time-to-failure tests.

Scanning Electron Microscopy of the Faults. Micrographs from the scanning electron microscopy (SEM) analysis are provided to illustrate several of the typical faults. Figure 4-30 is a micrograph of final test sample B. Figures 4-31 and 4-32 illustrate the typical fault of a break in the metal conductor at the transition. The arrows point to the breaks which are observed to occur frequently at the edge of the die. The two micrographs in Figure 4-33 illustrate the sharp edges (arrows) where the metal conductors fail to transition when the polyimide layer fails to properly planarize the surface. Figure 4-34 illustrates a failure at a via. Cracks occur at the bonding pad as shown by the arrows. Finally, defects occurring on the aluminum conductors are shown in Figure 4-35.

Discussion of the Test Results. Three final samples were evaluated. As a result of the initial continuity test, it was determined that the samples differed in quality. Sample A had a strong 82.3% yield. Sample C was second best with a yield of 66.7% and sample B was last at 61.1%.

Early Failures. All of the circuits that were found to have infinite resistance (continuity test) were labeled "early failures". There were 16 (of 54 circuits) early failures or 29.6% of the circuits. During the fault analysis (Table 4-XII), the causes of these early failures were determined. A net 56.3% of these early failures were due to a failure in the metal conductor as it crossed one or both of the gap regions or gap transitions. As seen in Figure 4-31 and Figure 4-32, cracks form along the width of the conductor. This fault typically

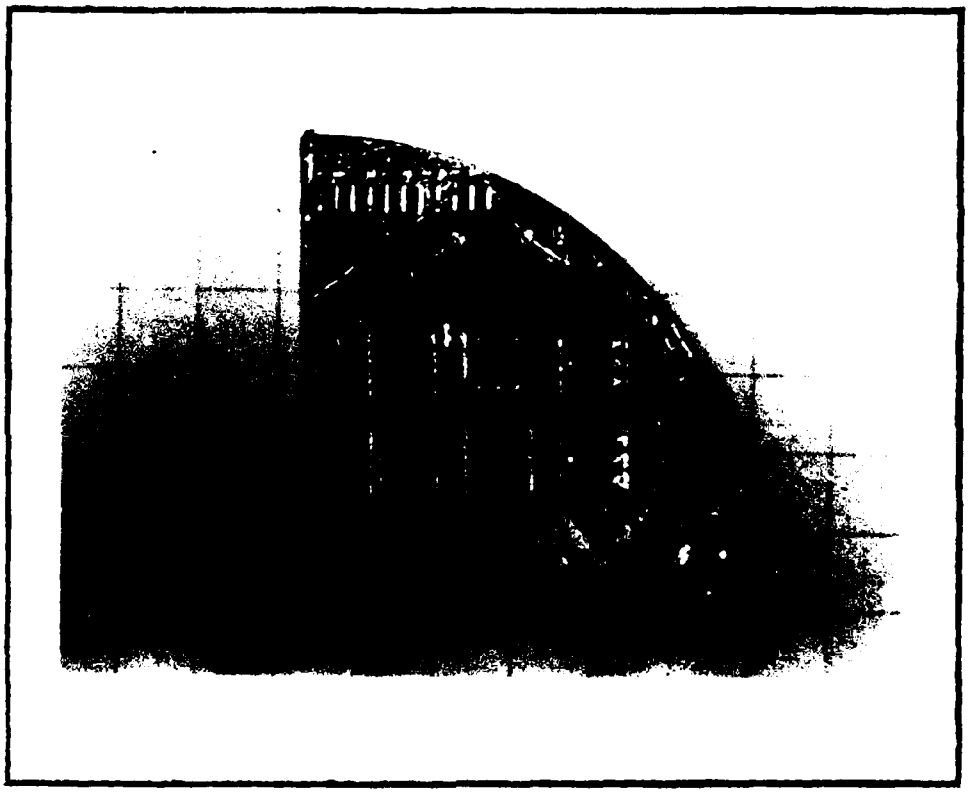


Figure 4-30. Photograph of Sample "B" After All Tests. The magnification factor is 1.66X.

Figure 4-31. SEM Micrographs of the Conductor Breaks Which Typically Occur at the Gap Region. (The arrows clearly mark the break in the metal.) The magnification factor is 325X.

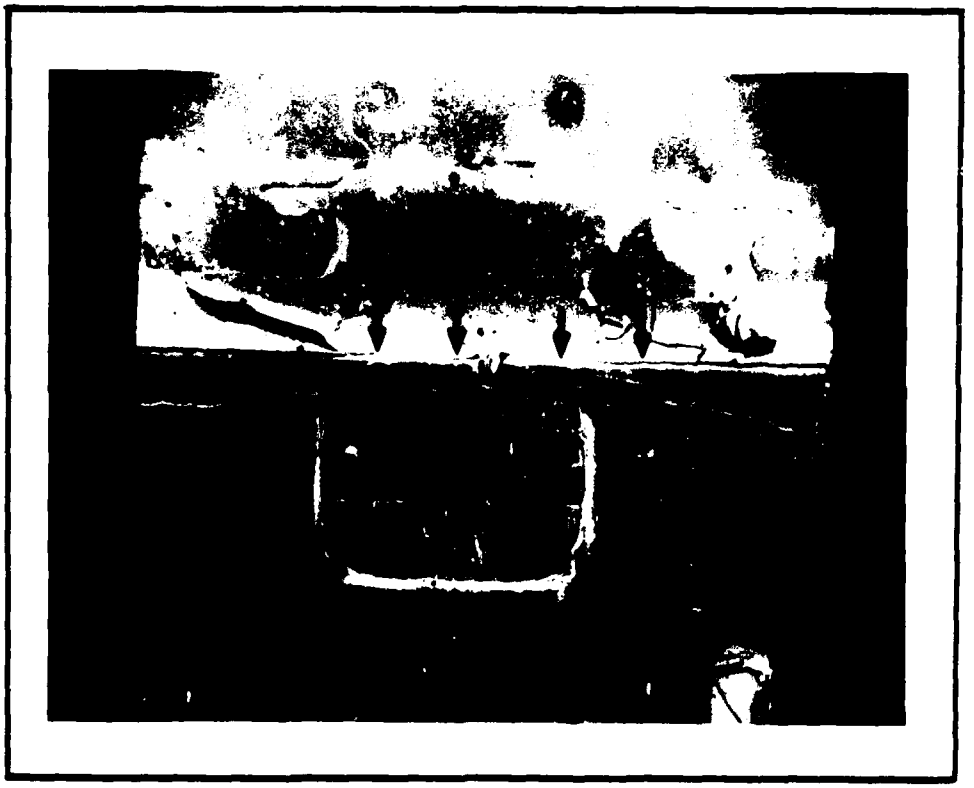


Figure 4-32. SEM Micrograph of the Conductor Breaks Which Typically Occur at the Gap Region (The arrows clearly mark the break in the metal.) The magnification factor is 125X.

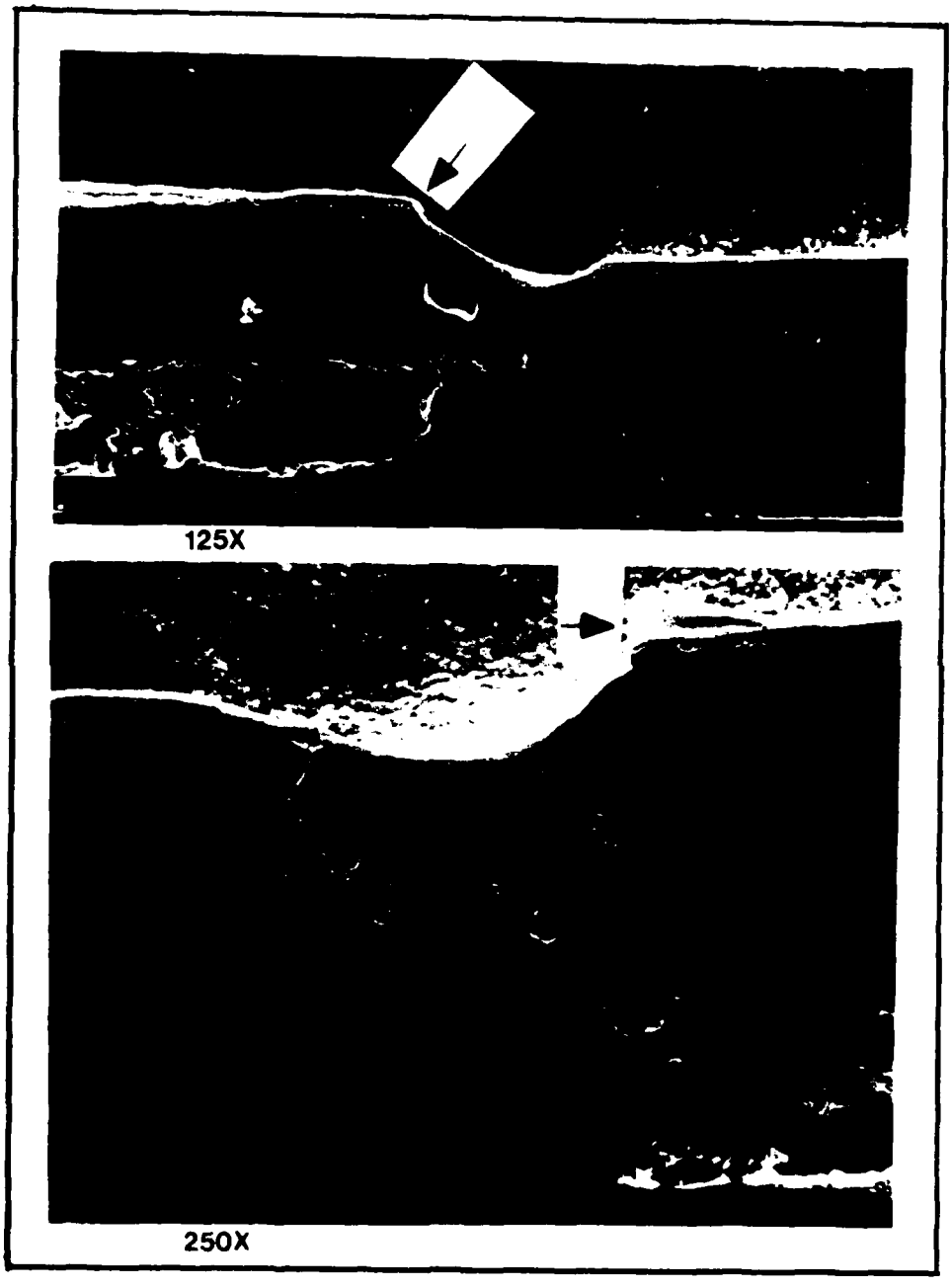


Figure 4-33. Cross-Sectional Micrographs of the Gap Region Showing Incomplete Planarization. (The arrows point to the sharp ridges which occur when the planarization is insufficient.) The magnification factors are shown.

Figure 4-34. SEM Micrograph of the Breaks Which Typically Occur at the Vias. (The arrows clearly mark the break in the metal.) The magnification factor is 250X.

Figure 4-35. SEM Micrograph of a Conductor Defect. Defects of this type occurred infrequently. The magnification factor is 20X.

occurs at the edge of the die. It is speculated that if the delta separation is large, the polyimide fails to properly planarize the sample's surface. Figure 4-33 shows how these sharp discontinuities will cause the metal coverage to be thin or non-existent at the die edge and thus, the circuit is open. The remainder (43.7%) of the faults were due to problems at the vias. Figure 4-34 illustrates how breaks occur in the aluminum at the interface of the bonding pad to the via metal. It is surmised that the breaks could be caused by either improperly sloping the via walls, or by contamination on the bonding pads of the die. It is noteworthy that almost all of the early failures in the overall statistics were attributable to via failure (all on sample B). Without sample B in the statistical sampling, there would be no failures due to improper vias. Perhaps sample B was contaminated during processing, or possibly, there was a slight departure from the via development procedure which caused sharply angled via sidewalls. It is apparent though, that most failures occurred due to breaks in the metal in the transition from the support substrate to the die.

Mean-Time-To-Failure (MTTF) Results. During the MTTF tests, 13 of the remaining 38 circuits (54 minus the early failures) or 34.2% failed. Almost all of these failures occurred due to cracks in the metal at the gap regions (11 of 13 or 84.6%). The remaining two failures were due to accidental loss of two circuits when a lab tool fell on them. Therefore, 5.3% of the sample lot was lost due to accidental failure.

Likely, the losses from the tests occur in circuits weakened as a result of the thin aluminum conductors at the die edges. The heat (150 degrees Celsius) accentuates the weaknesses at the transitions.

High Temperature Tests. The thermal tests at 350 degrees Celsius showed that the polyimide layer was not as stable as desired. The severe bubbling and blistering of the polyimide layer when exposed to that temperature, show the effects of not completely imidizing the layer. As long as the maximum processing temperature is limited to 250 degrees Celsius, the polyimide cannot be totally imidized (Figure 4-23). Consequently, excess heat could cause blistering of the layer at any time. It is interesting to note that even though the surface of sample C was completely blistered after the "rapid rate of temperature increase" test, only three of the circuits failed. Six of the 18 circuits survived all tests, including that test. The ramped temperature test had failures only when the samples reached the 275 degrees Celsius temperature. One failure occurred at 275 degrees Celsius and two at 325 degrees Celsius.

It was expected that none of the samples tested up to 350 degrees Celsius would have any surviving circuits. The test to determine the effect of the processing temperature showed that the die shifted an average of 70 microns when exposed to a 350 degree Celsius temperature. It was expected that the shifting would have caused breaks in all of the remaining conductors transitioning the gap regions. Of the circuits tested at 350 degrees Celsius, only 22.7% of them failed. Either the expected swelling did not occur or the circuits survived in spite of the swelling. A possible explanation is that the polyimide layer compensates for the shifting of the die. The elasticity of the polyimide layer allows the conductors to remain intact as the die rise due to the heat

Summary. The performance tests revealed that the process is fairly successful. A 46.3% lot of the circuits survived all tests. This percentage increases when the early failures are removed from the

statistics. Twenty-five of the circuits survived. Of the 38 circuits tested, this represents 65.8% of the total lot. The major failure mode was the cracking of the aluminum conductors at the die edges. It is speculated that this failure mode is due to insufficient planarization over a large delta separation.

V. Conclusions And Recommendations

Before concluding remarks are made, the problem statement from Chapter I is restated: "This study investigated a silicon-hybrid method of Wafer Scale Iintegration which involves mounting discrete integrated circuit die into etched "wells" of a supporting silicon wafer, aligning the top surfaces of the die and the support substrate, planarizing the gap between the die and the substrate, applying a conformal dielectric smoothing layer, and then interconnecting the circuit die using a patterned thin film metallization technique. The study seeks to establish a fabrication process by which electrically tested integrated circuit die can be close-mounted and reliably interconnected with relatively low impedance micro-strip conductors." To determine whether or not these objectives were met, each step of the process (using descriptive phrases from the problem statement as a guide) is addressed the following discussion.

Conclusions

A silicon-hybrid wafer scale integration process been demonstrated in this research effort. The initial yield of functioning circuits (61.4%) indicates that the process is viable. For use in mounting actual integrated circuits, however, further research will be needed to optimize the process. Conclusions concerning the individual steps involved in the process are given in the following subsections.

Etching "Wells" Into A Supporting Silicon Wafer. The wet orientation dependent etching (WODE) study was accomplished to determine the optimal [illegible] wafer and etchant combination for etching the wells needed for [illegible] the integrated circuit die. The combination recommended for

fabricating the final test samples was (100) oriented silicon wafers and the potassium hydroxide, isopropyl alcohol (buffering agent), and deionized water etchant. The results obtained were very satisfactory. This combination yielded smooth, flat well bottom surfaces that were etched with excellent control. The major disadvantage encountered was the angle (50 degrees) of the well's sidewalls. Since the sidewalls characteristically etch with an angle of approximately 50 degrees with respect to the plane containing the well's bottom, the gap surrounding the die is approximately 7 mils wide at the well's top surface. With this choice of silicon orientation and etchant, the major problem to surmount in the subsequent research was how to achieve reliable conductor interconnection across this gap. The (110) silicon did not show promise for this process because the resulting well bottoms were heavily striated and the well's perimeter etched into a rhomboidal shape.

Mounting Discrete Integrated Circuit Die. The results of the die attach adhesive study indicated that the Master Bond EP-34CA Special two-component epoxy was the adhesive of choice for fabricating the final test samples. However, one conclusion formulated from the evaluation of the final test samples, was that this adhesive may not be appropriate for the HWSI process. The delta separation measurements made in the process temperature effects evaluation indicated that the die "shell" and [illegible] out of a perfectly aligned position [illegible] delta separation when exposed to heat. This is likely due to pressure building under the die as the adhesive outgasses. Temperatures of [illegible] degrees celsius caused delta separations in the range of [illegible] to [illegible] microns. The large delta separations observed to cause early failure [illegible] due to cracks in the metal conductors. These cracks were observed to occur at the die edge [illegible]

uted to insufficient planarization. The processing temperature effect tests led to the conclusion that the maximum tolerable processing temperature for this adhesive should be limited to 250 degrees Celsius. Higher temperatures led to rapid swelling of the adhesive. This relatively low processing temperature severely limits the degree of imidization of the polyimide layer. Another adhesive choice may be needed to rectify the disadvantages of the EP-34CA epoxy. Alternatively, another course of action to solve the problem of the die swelling upward (due to outgassing), would be to etch small holes in the bottom of the well for the gases to escape. These two solutions are discussed in the Recommendations subsection in this chapter.

Aligning The Top Surfaces. The technique for aligning the top-surfaces of the die and the support substrate is simple, yet labor intensive. The tests implemented to determine the effect of the processing temperature on the delta separations, indicated that the die had risen and shifted in their wells from 30 to 50 microns after their cure cycle. This swelling is due to deficiencies in either the alignment technique or in the adhesive (or both). Follow-on research needs to be accomplished to determine the role of the alignment procedure in these initial delta separations.

Planarizing The Gap. One of the advantages of using the two-component epoxy as a die attach adhesive is that the excess adhesive under the die will flow into the gap regions surrounding the die and thus fill them. This behavior partially planarizes the top surface of the sample. A meniscus forms at the top surface of the epoxy due to shrinkage during cure. However, the polyimide planarizing layer compensates for these slight discontinuities and promotes the planarization of the top surface.

Overall, the EP-34CA epoxy is an excellent void filler with a thermal coefficient of expansion matched to silicon. A significant disadvantage is that voiding is possible in the gap if the epoxy is not cured gradually and the shrinkage compensated for with additional layers. Overall, the epoxy is well adapted to fulfill this function in the fabrication process.

Application of the Conformal Dielectric Smoothing Layer. The photosensitive polyimide (Merck Selectilux HTR 3-200) provided an excellent coating which planarized the surface of the wafers. Cross-sectional photographs of the gap regions planarized with the polyimide, demonstrated the material's capability for smoothing the transition between the support substrate and the IC die. Additionally, it's photosensitive features eliminated several processing steps typically associated with etching vias in traditional polyimide layers. This polyimide is well suited to the needs of the HWSI process.

Interconnecting The Circuit Die. The evaporation and patterning of the aluminum interconnections followed the standard IC processes. The results of these steps yielded adequate conductors.

Recommendations.

To further optimize the HWSI fabrication process, several areas should be explored. Specific recommendations are discussed in the following paragraphs.

Characterization of the Silicon Substrate Etching. It is recommended that research be conducted to further characterize the (100) silicon and KOH-DIW-IPA etchant combination. Etch rate versus etchant temperature experiments should yield greater knowledge and control over the etch process. The "pyramid" defects should be investigated. Knowledge of their

cause and a means of preventing them would be beneficial to the HWSI process.

In future etching trials, it is recommended that a quartz reflux condensing system be used. The stainless steel vessel used for the trials in the WODE study and subsequent etching, did not allow for precise temperature control of the etchant. Also, the primitive reflux condensing cover permitted the escape of a small amount of water vapor. During the 4 hour (or more) etching trials, sufficient water and isopropyl alcohol escaped to seriously affect the etchant concentration. This of course, changed the etching rate and quality of the results. The behavior of a quartz condenser should greatly enhance the etching results. It is also recommended that fresh etchant be used for every etching trial. Expended etchant yielded poor quality well bottoms.

Maximum Processing Temperature. The limited maximum processing temperature of 250 degrees Celsius significantly impacted the overall results. A higher processing temperature will facilitate a greater degree of polyimide imidization. Further, a higher temperature will allow for more effective annealing of the aluminum conductors. This impact may be best realized at the via interconnections to the bonding pads. If VLSI or VHSIC chips can withstand a 350 degree Celsius temperature without their electrical characteristics being changed, then this HWSI process could be enhanced by using cure and anneal cycles at that level.

Investigation of Die Attach Adhesives. Research should be conducted to investigate alternate die attach adhesives. The two-component epoxy swells unacceptably when heat is applied. An adhesive with minimum outgassing is needed to solve this problem. Since the DAA study was conducted, literature on other adhesives has been obtained. One promising

adhesive is the Conductimer (M & T Chemicals Inc., Rahway, NY) thermoplastic adhesive (19:38). This adhesive is a siloxane polyimide compound which offers rapid bonding times spanning a wide range of cure temperatures. This product is available in tape form which could be beneficial to the HWSI process. Square tape pieces (195 mils by 195 mils and 1.5 mils thick could be sandwiched between the bottom of the IC die and the top surface of the well. The cover glass and weight technique could be used with a modified variation. The weight needs to be 200 grams and the bonding temperature should be 350 degrees Celsius. The thermoplastic adhesive has a characteristic low residual stress which compensates for thermal mismatch between materials. The adhesive is suitable for complex, multichip assemblies because rework is possible. That is, defective devices can removed by the application of a local heat source and easily replaced (before application of the conformal polyimide layer).

Another family of adhesives which are recommended for evaluation are the polyamic acid adhesives. Several manufacturers have adopted these products because of their higher thermal endurance (19:37). The polyamic acid products have demonstrated significant reliability. One potential disadvantage is their high moisture content (19:38).

A Proposed Alignment Technique. The following alignment technique is recommended for investigation. To relieve the gasses generated in the adhesive during cure (which cause the IC die to "swell" out of position), a number of small passages (etched from the back of the wafer through the well bottoms), could be fabricated using the same anisotropic etch techniques realized in the WODE study. This etching process could be accomplished after the wells are etched. A matrix (perhaps 4 x 4) of these channels could be placed at the bottom of each well. The channels might be

approximately 20 mils square at the well bottom. Further, it is recommended that the die/wafer samples be cured "upside down". By first mounting the IC die with the technique described in the DAA study (Chapter III), the samples could then be inverted so that the die's top surface is facing downward. The samples would be cured in this position, allowing gravitational forces to align the die to the support substrate. Excess epoxy and gasses will flow out of the etched channels as the sample is cured. Instead of placing the sample on a glass flat, a teflon block should be used to prevent the sample from adhering to the alignment surface as it cures. This technique would allow the fluid epoxy to flow to the teflon alignment block and solidify without the meniscus forming. A ramped cure cycle is recommended to assure a minimum of outgassing. Figure 5-1 illustrates the proposed bonding process.

Goals of Future Research. This research project was a pioneering investigation of materials and processes to determine the feasibility of silicon-hybrid wafer scale integration. In order for further research to address current packaging needs for high speed computational systems, the conductors will need to be much narrower and thinner. This trend should be incorporated in future work. Experimental testing should be accomplished to determine the minimum design geometries and the minimum metal thickness. The via sizes need to be reduced, and the planarizing polyimide layer needs to be made thinner. It is recommended that follow on projects utilize operational integrated circuits (at least, small scale integration) which can be electrically interconnected and operated

Summary of Conclusions And Recommendations

The results of this evaluation demonstrated that the proposed HWSI

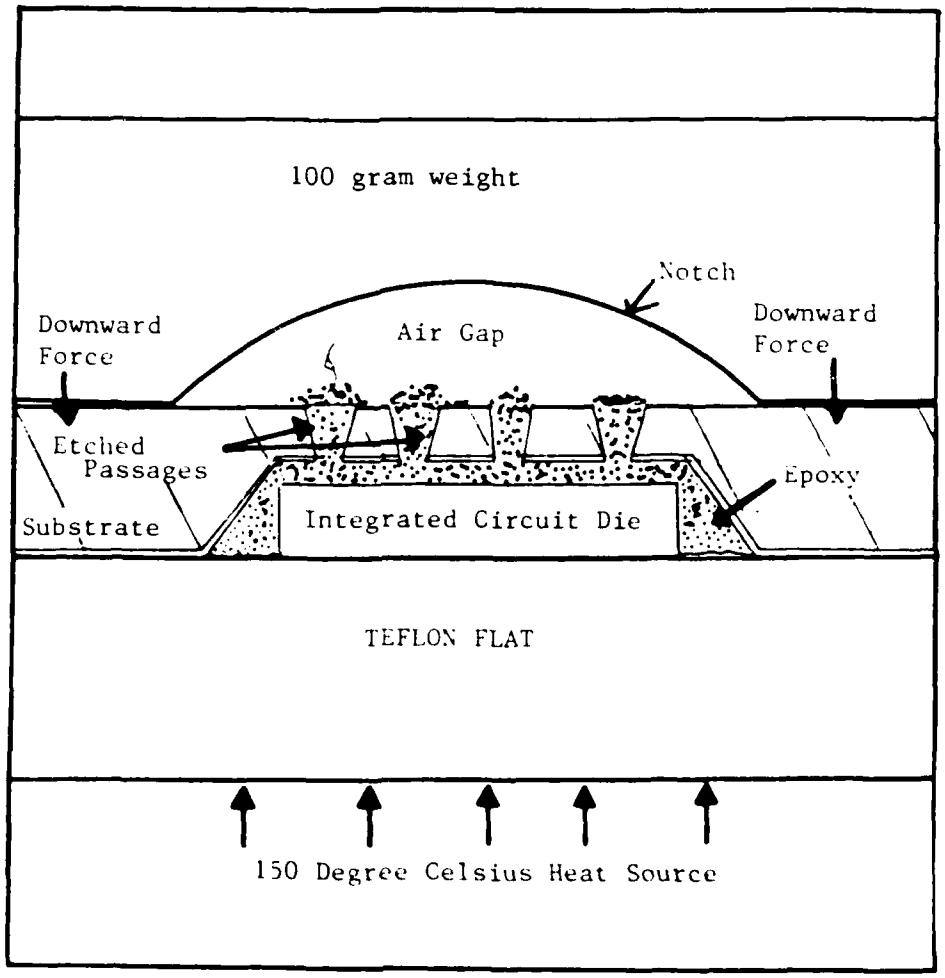


Figure 5-1. The Proposed Bonding Technique.

process is viable, and further research can enhance its potential. The fundamental problem is the delta separation between the mounted die and substrate. Materials and techniques need to be further investigated to provide die bonding that aligns the die with the surface of the silicon substrate and does not permit movement when heat is applied.

Appendix A: Silicon Crystal Structure and Notation.

The three basic families of planes (and their orthogonal directions) in single crystal silicon are presented in Chapter II. This supplemental material describes the various angles these planes make with respect to each other. These angular relationships were manifested during the anisotropic etching experiments.

Angles Between The Three Basic Families of Planes. Silicon in its crystalline state forms the diamond lattice structure. The diamond lattice structure is illustrated in Figure A-1. The figure illustrates how interpenetrating cubic structures. An analytical relationship is presented by Cullity (36:460) for calculating the angle between the various planes in a cubic-crystal structure (the silicon crystal structure is a specific case). That is,

$$\theta = \cos^{-1} \left((h_1h_2+k_1k_2+l_1l_2) \; / \; [(h_1^2+k_1^2+l_1^2)(h_2^2+k_2^2+l_2^2)]^{1/2} \right) \quad \text{(A-1)}$$

where θ is the angle between two planes $(h_1k_1l_1)$ and $(h_2k_2l_2)$. The two planes are defined by the Miller index notation. Using this formula, the following angular relationships between the planes (100), (110), and (111) (and their equivalent planes), can be calculated.

(100) Orientation Silicon. In (100) wafers, the plane of the wafer is one of the {100} planes and one of the <100> directions is normal to the plane of the wafer's surface. The primary wafer flat is one of the {110} planes. When anisotropical etching takes place, the silicon atoms in the {111} planes are the slowest to be removed because these planes have the largest atomic density. Therefore, the intersections of the {100} planes with the {111} planes and the intersections of some of the

{100} planes with each other, are of prime importance when analyzing (100) orientation silicon. When {100} planes intersect {111} planes, only two angles result from equation (1). The denominator of this combination is always the square root of 3. The numerator is either 1 or -1. The inverse cosine of $(3)^{-(1/2)}$ is 54.7 degrees and the inverse cosine of $-(3)^{-(1/2)}$ is 125.26 degrees (the complement of 54.7 degrees). All intersections of the planes in the {100} family are at 90.00 degrees. This is why the sidewalls theoretically form at 54.7 degrees. Therefore, when using (100) silicon and aligning the square well pattern to the wafer flat (which should be be the (110) planes), the sidewalls will always be 54.7 degrees or 125.2 degrees in relation to the well bottom (which is also a {100} plane). This angular relationship is illustrated in Figure A-2.

(110) Orientation Silicon. In (110) wafers, the plane of the wafer is one of the {110} planes and one of the <110> directions is normal to the plane. The primary wafer flat is one of the {111} planes. When anisotropical etching takes place, the silicon atoms in the {111} planes are slowest to be removed because this plane has the largest atomic density. Therefore, the intersections of the {110} planes with the {111} planes and the intersections of some of the {111} planes with each other, are of prime importance when analyzing (110) orientation silicon. When {110} planes intersect {111} planes, three angles result from equation (1). The denominator of this combination is always the square root of 6. The numerator is either 2, 0, or -2. The inverse cosine of $[2 / ((6)^{-(1/2)})]$ is 35.3 degrees and the inverse cosine of $[-2 / ((6)^{-(1/2)})]$ is 144.7 degrees (the complement of 35.3 degrees). The inverse cosine of 0 is 90 degrees. Thus, these three combinations yield

angles of 35.3 degrees, 144.7 degrees (the complement of 35.3 degrees) or 90.0 degrees. For this reason, when anisotropically etching <110> silicon, the sidewalls are either 90.0 degrees or 35.3 degrees. This angular relationship is illustrated in Figure A-3.

The individual members of the {111} family of planes can intersect each other at four different angles. The demoninator of equation (1) with this combination is always 3. The numerator can be either -3, -1, 1, or 3. The corresponding angles formed are the inverse cosines of 0.33, and -0.33. The resulting angles are 70.5 degrees and its complement, 109.5 degrees. The individual planes in the <111> family of planes, do not intersect each other at 90 degrees as do the {100} planes. This explains why in (110) anisotropic etching, the rectangular oxide masks yield rhomboid shapes. The corners are not square; the etched planes intersect at 109.5 degrees.

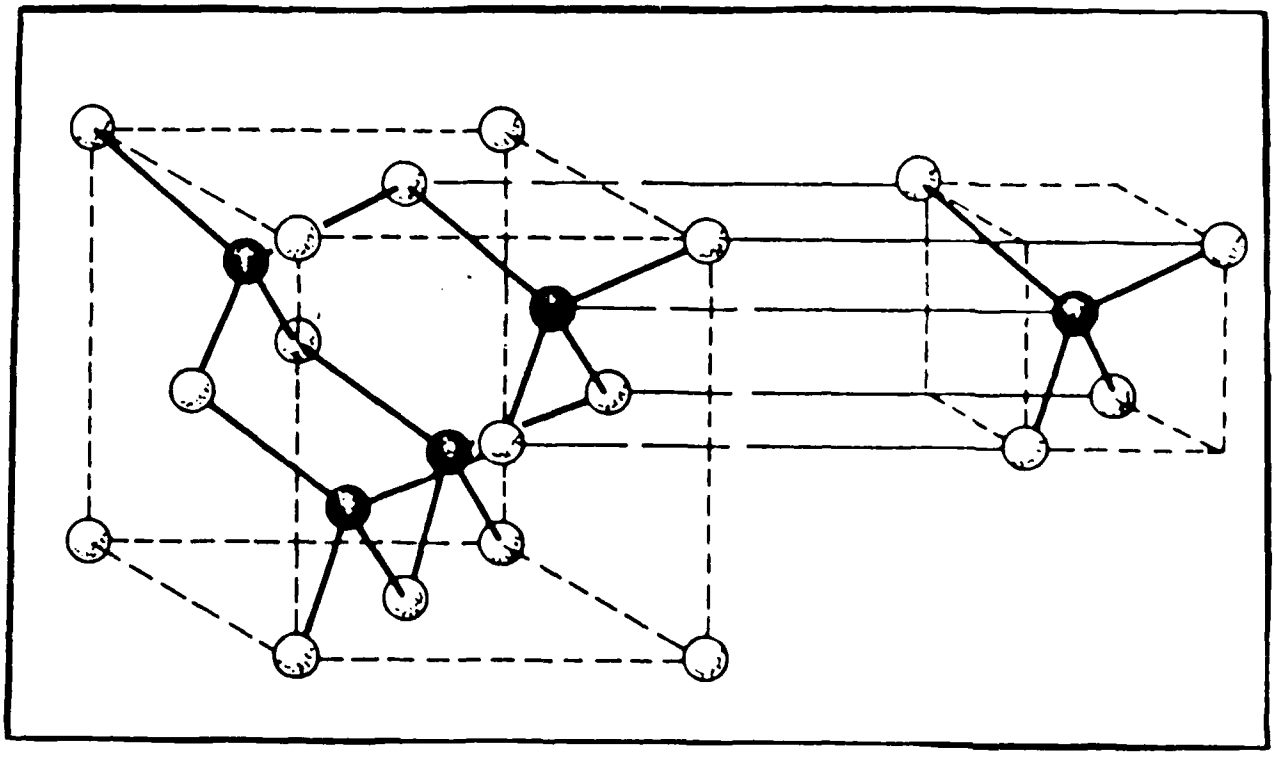


Figure A-1. The Diamond Lattice (37:53).

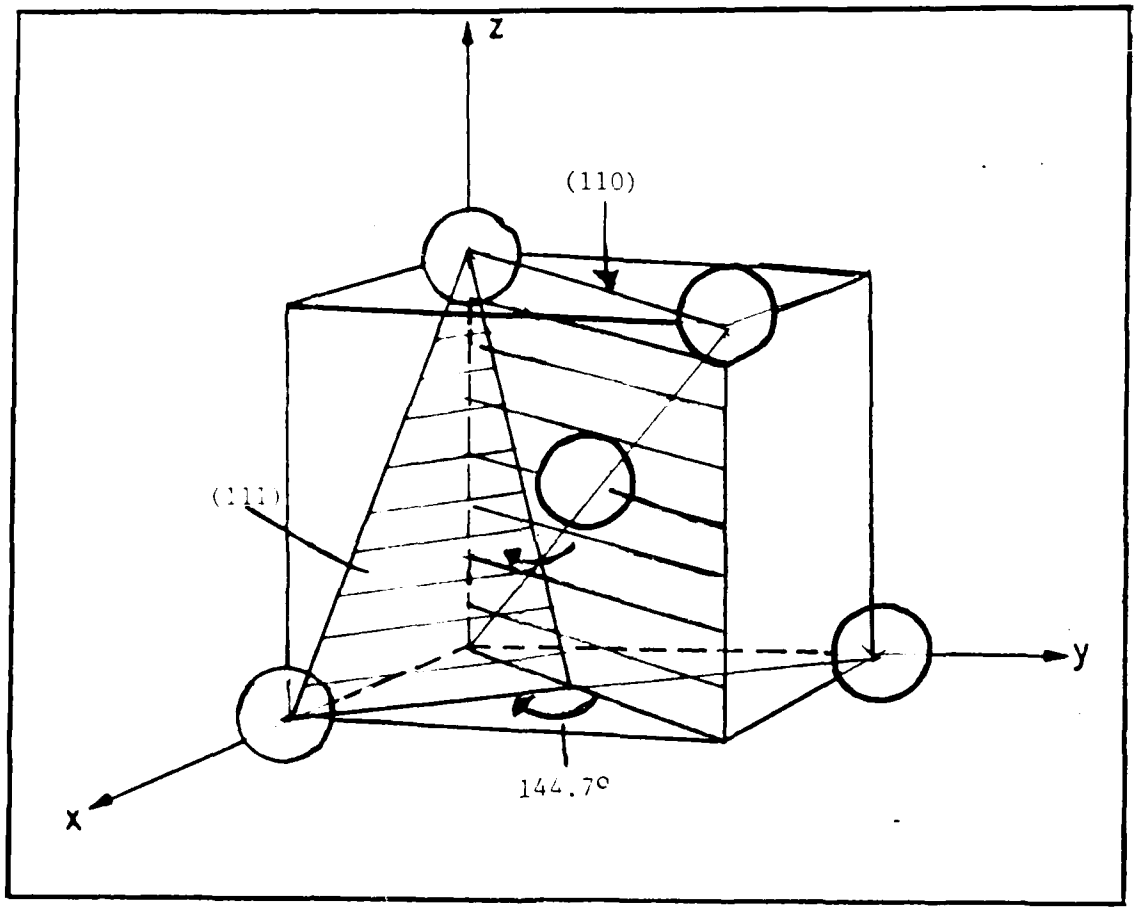


Figure A-2. The Angle Between the (100) and (111) Planes in a ... Crystal Illustrated.

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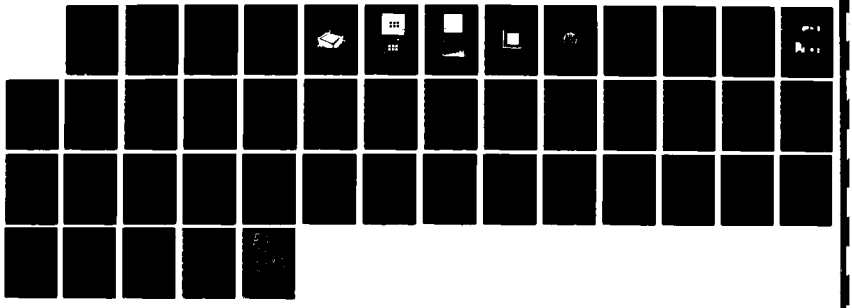
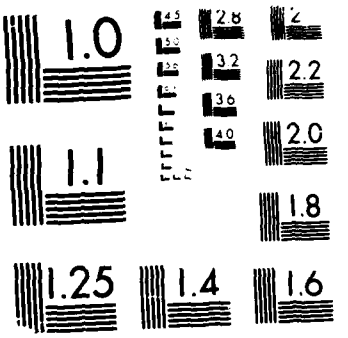




MICROCOPY RESOLUTION TEST CHART

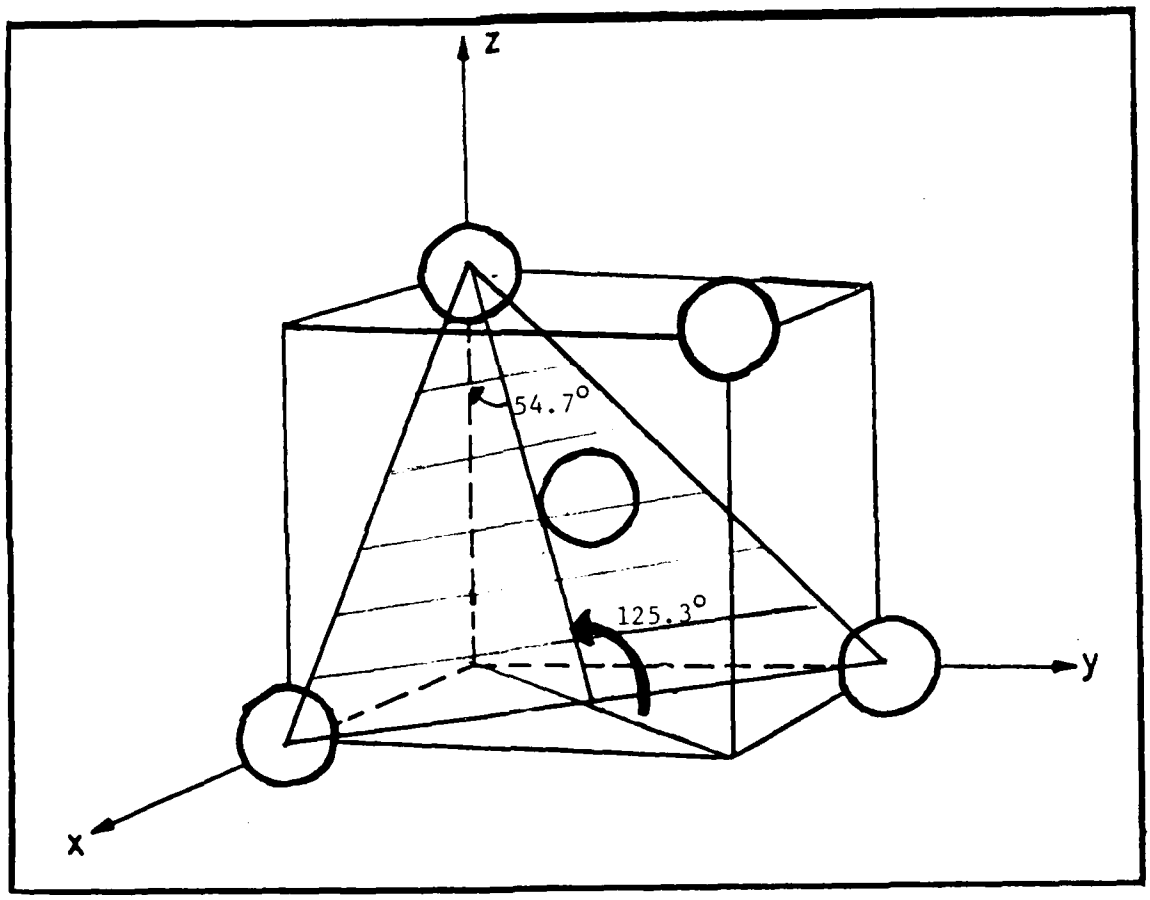


Figure A-3. The Angle Between the (110) and (111) Planes in the Cubic Crystal Illustrated.

Appendix B: The Mask Fabrication Process

Equipment and Materials. The following equipment was used in the mask fabrication process:

1. X-Y plotting and cutting table (also known as the Coordinotograph). The Coordinotograph is illustrated in Figure B-1.
2. Knife for cutting the rubylith.
3. Mask Camera (Model 6720, Dekecon HLC Engineering Co., Oreland, PA).
4. Photoplate development unit which consists of five stainless steel tanks which hold the photographic development chemicals.

The following materials were used in the mask fabrication process:

1. Rubylith (Stock number 263514, Ulano Corp.,Brooklyn, NY; size: 40 inch wide roll).
2. Kodak High Resolution Photoplates (HRPs); size: 2" x 2".
3. Kodak photoplate development chemicals.

Procedure. The following procedure was used to generate the photolithography masks for the Wet Orientation Dependent Etching (WODE) study and the preparation of Hybrid Wafer Scale Integration (HWSI) samples.

A design was drawn full scale on a large sheet of rubylith. The pattern used in the WODE study consisted of a two-by-three matrix of squares. The size of the squares on the mask needed to be 200 mils square. Therefore, the rubylith was cut to produce a pattern that was 4 inches square. (Assuming a 20X reduction of the mask camera, this will yield a 200 mil square shape on the actual mask.)

The rubylith was then photographed using the mask camera. The reduction multiplier for these masks was 20X. The exposed photoplates were developed using the standard development process. Complete information on the development of high resolution photoplates is available at the AFIT Cooperative Materials and Electronic Processing Laboratory.

Masks Used In This Research Project. The masks designed, fabricated, and used in this research project are illustrated in the following figures:

1. Figure B-2 Photomask of the Well Pattern.
2. Figure B-3 Photomask of the Vias Pattern.
3. Figure B-4 Photomask of the Die Pattern.
4. Figure B-5 Photomask of the Second Level Metallization Pattern.

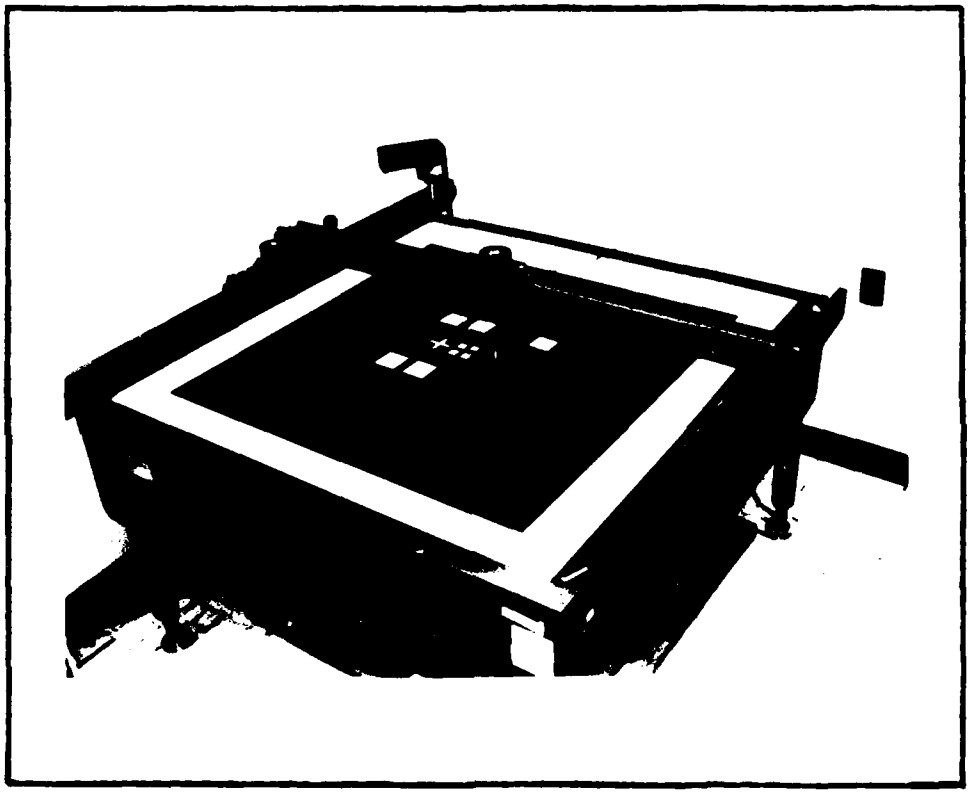


Figure B-1. Coordinatograph Photomask Plotting and Cutting Table.

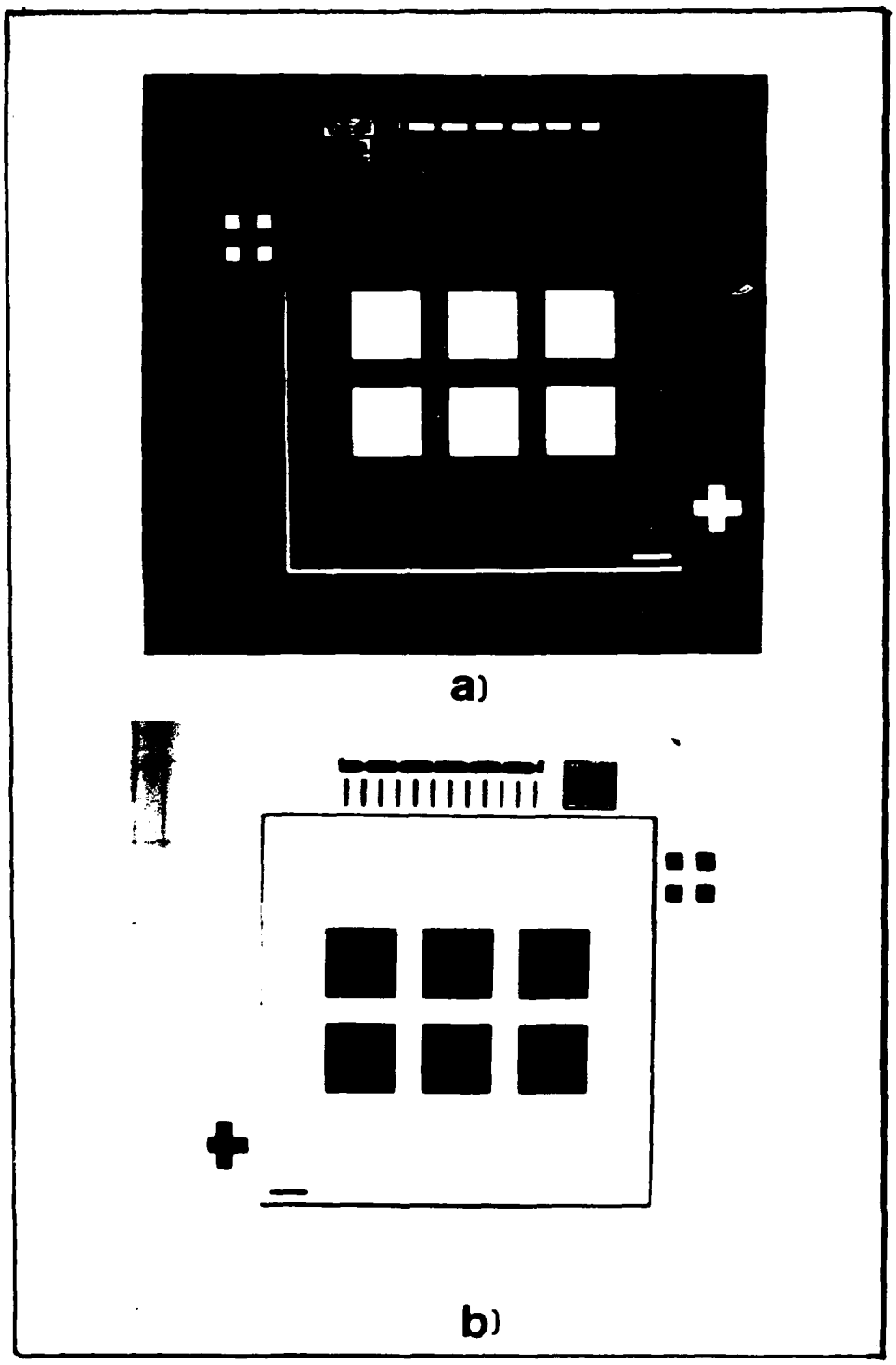


Figure B-2. Photomask of the Well Pattern.
a) Positive mask.
b) Negative Mask. (The mask is laying on graph paper with 0.250 inch grid.) The magnification factor for both photographs is 1.6X.

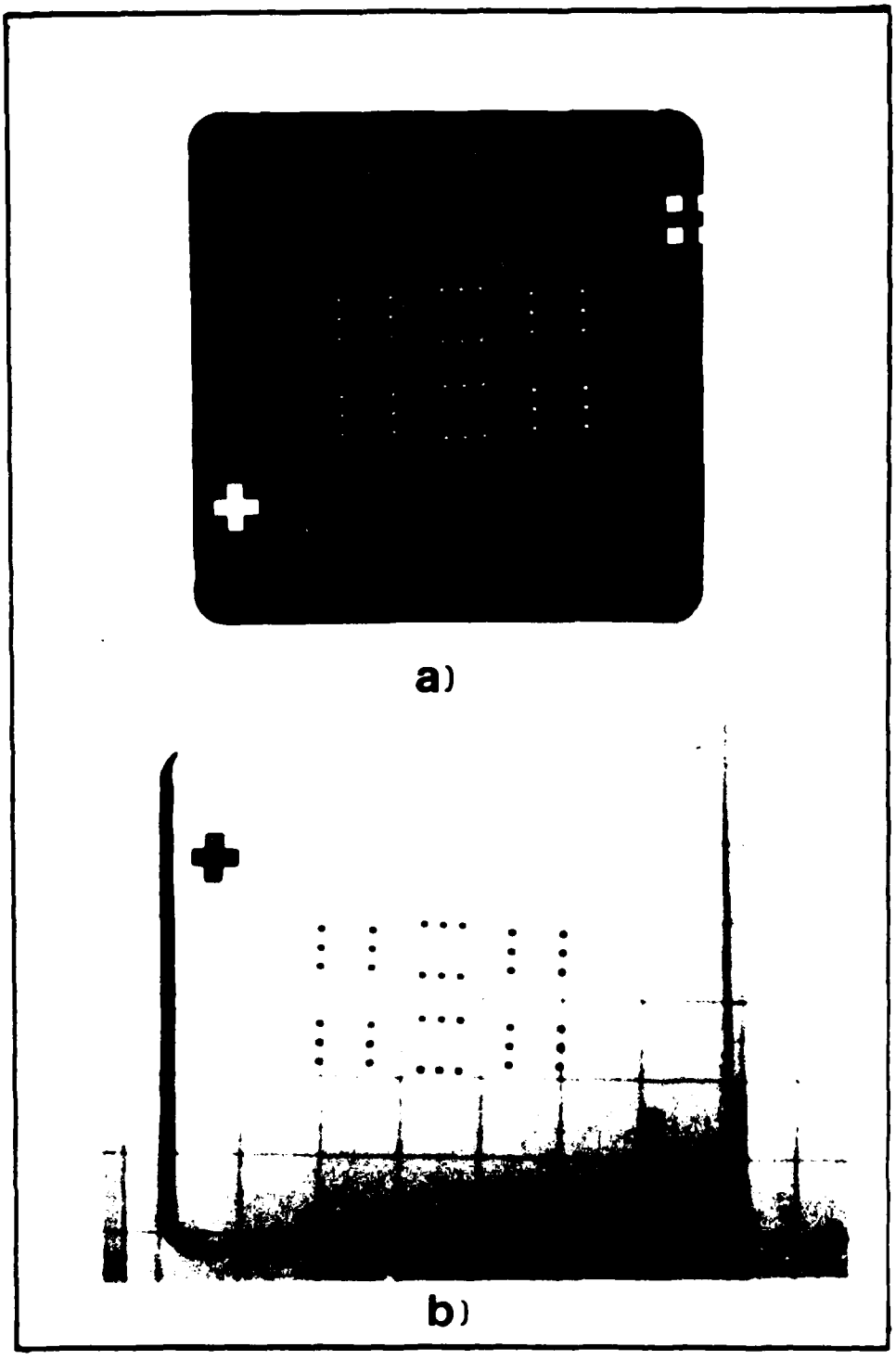


Figure B-3. Photomask of the Via Pattern
a) Positive mask
b) Negative Mask. (The mask is laying on graph paper with 0.250 inch grid.) The magnification factor for both photographs is 1.6X.

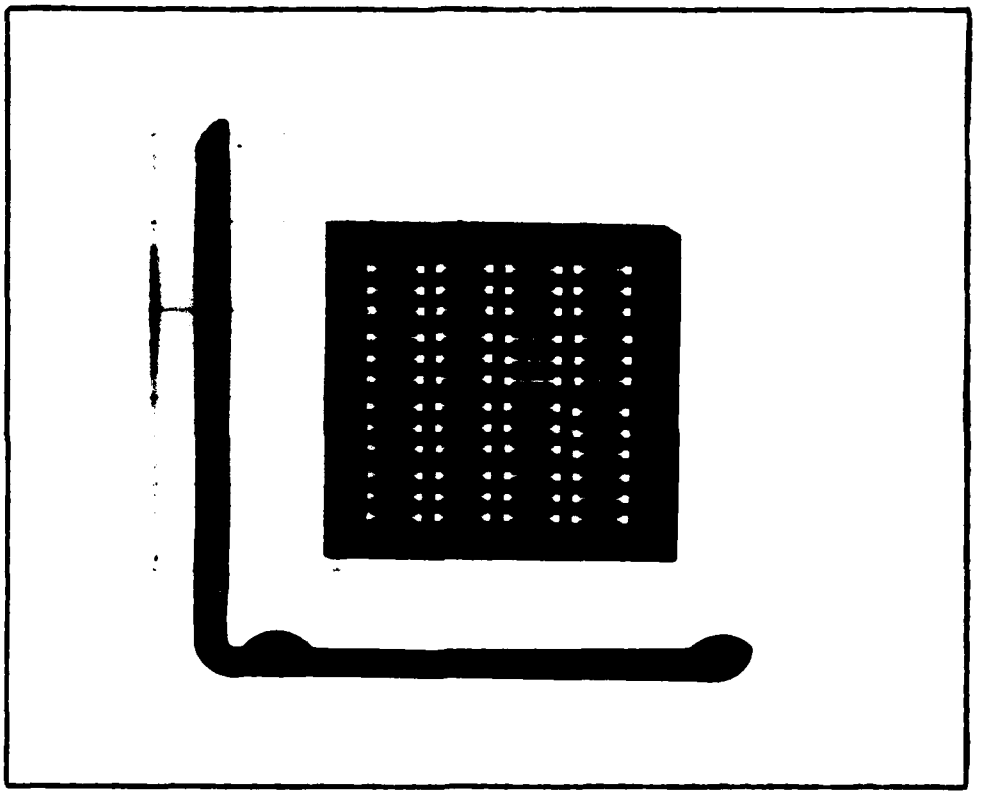


Figure B-4. Photomask of the Die Pattern. (The mask is laying on graph paper with 0.250 inch grid.) The magnification factor is 1.6X.

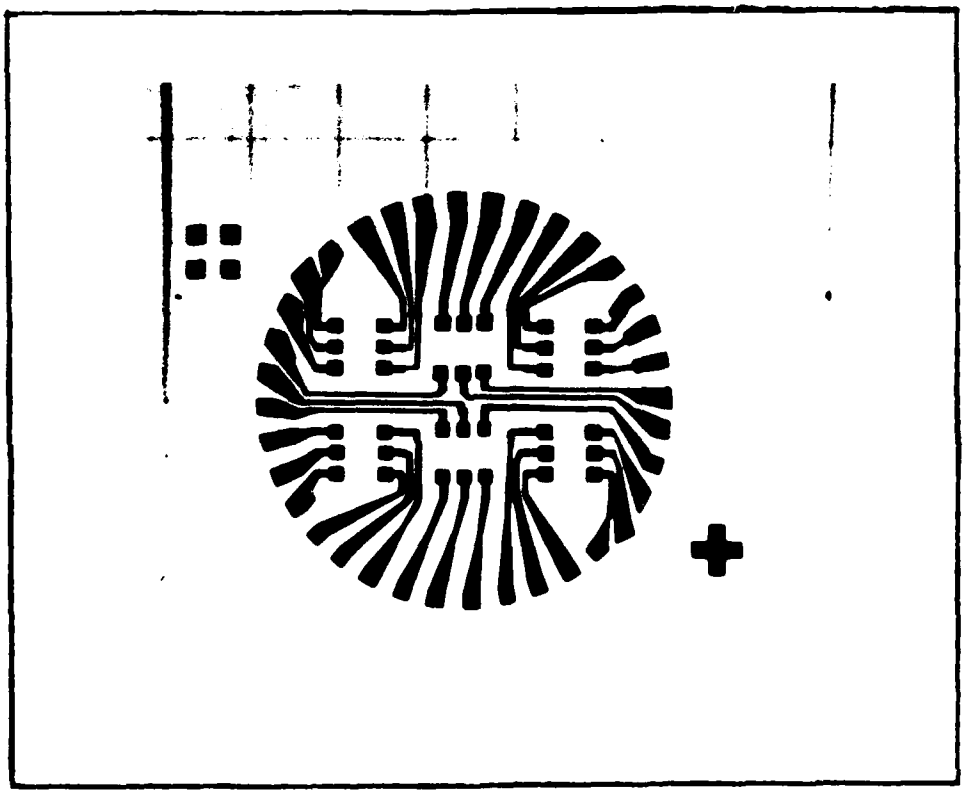


Figure B-5. Photomask of the Second Level Metallization Pattern. The magnification factor is 1.6X.

Appendix C: Oxidation and Masking of Silicon Wafers

Equipment and Materials. The following equipment was used to prepare the wafers for the etching study:

1. Labware for the standard clean procedure.
2. Thermal oxidation furnace with quartzware.
3. Photoresist (PR) spinner.
4. Prebake and postbake ovens (70 - 220 degrees Celsius).
5. Labware for oxide etching and PR development.

The following materials were used in the preparation of wafers for the etching study:

1. Chemicals for Standard Clean #1: Sulphuric acid (H_2SO_4)
   Hydrogen Peroxide (H_2O_2)
   Hydrofluoric Acid (HF)
2. Silicon wafers: (Four types of wafers were used in this research):
   a) <110> 0.875 inch diameter n-doped wafers for the <110> combinations.
   b) <100> 1.25 inch diameter n-doped wafers.
   c) <100> 1.25 inch diameter n-doped wafers.
   d) <100> 3 inch diameter p-doped wafers which were quartered into four equal pieces. The last three types were used in the <100> runs. The quartered 3 inch wafers were 20 mils thick, and they used in extended etch trials.
3. Negative photoresist (Waycoat IC Resist, Type 3, 28 and 43 cps) and positive photoresist (Shipley Microposit 1350J).
4. Developer chemicals for the photoresists.

5. Buffered hydrofluoric acid for etching windows in the oxide mask.

Procedure For Oxidizing the Wafers. The wafers were prepared for the etching study by first cleaning them using the Standard Clean #1 procedure to remove contaminants (Appendix D). The clean wafers were placed vertically in a quartz boat for oxidation. To begin the oxidation process, the boat was slowly inserted (at a rate of 1 inch per minute for the first 12 inches; then 5 inches per minute for the remainder of the distance to the center of the tube) into the oxidation furnace and subjected to a dry-wet-dry cycle. The initial dry oxidation phase lasted 10 minutes; the wet period ranged from 4 to 12 hours depending on the thickness of the oxide desired, and the terminal dry period spanned 10 minutes to 60 minutes. The wafers were then slowly removed from the tube (rates opposite those for inserting the wafers into the tube). The exact process times for a particular wafer used in a specific trial are posted on the data sheets presented in Chapter IV and in Appendix E. Once oxidized, the wafers were stored under nitrogen in a closed container. When the oxidized wafers were needed, they were prebaked (250 degrees Celsius) to drive off moisture. After cooling to room temperature, they were coated with photoresist.

Procedure For Patterning the Oxidized Wafers. Positive photoresist was spun on the oxidized wafer's surface at 5000 rpm and prebaked for 20 minutes at 70 degrees Celsius. Hexamethyldisilazane (HMDS), an adhesion promoter, was used with the positive resist. The process was repeated for the back side of the wafer with one variation; the photoresist was swabbed onto the wafer back. This procedure was implemented to protect the oxide on the wafer's backside.

Using the appropriate mask, the wafers were then exposed to ultraviolet (UV) light for 45 seconds (4.0 mWatt/cm^2/second). The masks used in the project are illustrated in Appendix B. Because the features on the masks are relatively large, a automatic mask aligner could not be used to expose the photoresist on the wafers. A manual mask alignment tool was fabricated and is illustrated in Figure C-1. The photoresist coated wafers were placed on the tool with the flat coinciding with the alignment marks on the stage. The mask was placed on top of the wafer (Figure C-1 illustrates how the mask is rotated on and off the wafer), and the entire stage placed under the UV source for exposure. The UV source was the Cobilt Contact Printer and Mask Aligner. The stage was placed in the column of UV light, and the exposure duration was controlled by the settings on the contact printer.

After exposure, the wafers were developed. The photoresist development was accomplished by spinnig the wafers at 1000 rpm while spraying the surface with a 1:1 Shipley Microposit D312 developer-deionized water solution for 20 seconds. As the spinner continued to spin, the surface were rinsed with deionized water for another 20 seconds. Finally, the surface was blown dry with a nitrogen gas purge. The wafers were then placed in a forced air oven set at 120 degrees Celsius for post-baking (30 minutes).

Procedure for Etching the Oxide. At this point, the wafers were completely protected by photoresist except for the particular mask pattern on the topsurface. The wafers were then immersed in a buffered HF solution (6:1 NH_4F:HF) to etch the mask windows through the oxide, and thus, exposing the bare silicon substrate for later anisotropic etching. The etch duration required in the buffered HF solution was a

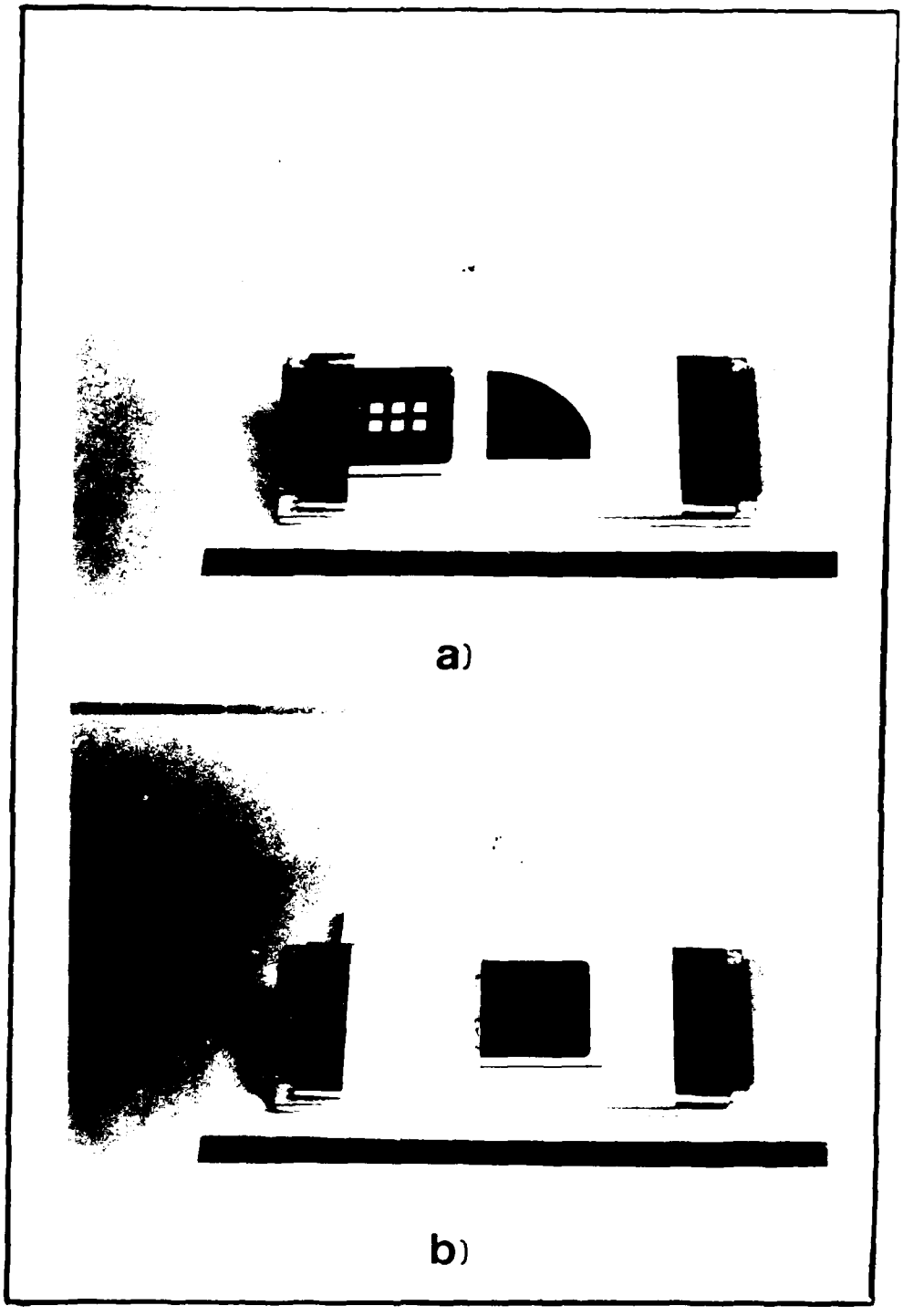


Figure C-1. Manual Mask Alignment Tool.
a) Quartered 3 inch wafer is placed on the stage with the flat aligned with the alignment marks on stage. The mask was hinged with tape. b) The mask is rotated back in position on the top of the wafer (coated with photoresist) and is ready for ultraviolet light exposure.

function of the etchants temperaure and the thickness of the oxide masks. The wafers were removed from the solution each minute to visually assess the etching progress. After the oxide windows were observed to be clear of any oxide, the wafers were placed in a deionized water (DIW) rinse for 20 minutes. The postbaked positive photoresist was removed by immersing the wafers in an ultrasonic bath of acetone for 15 minutes. The wafers were again rinsed in DIW for 20 minutes, blown dry with nitrogen gas, and placed in a convection oven (150 degrees Celsius) until needed for use.

Appendix D: Standard Cleaning Processes

Standard Clean 1 (SC1)

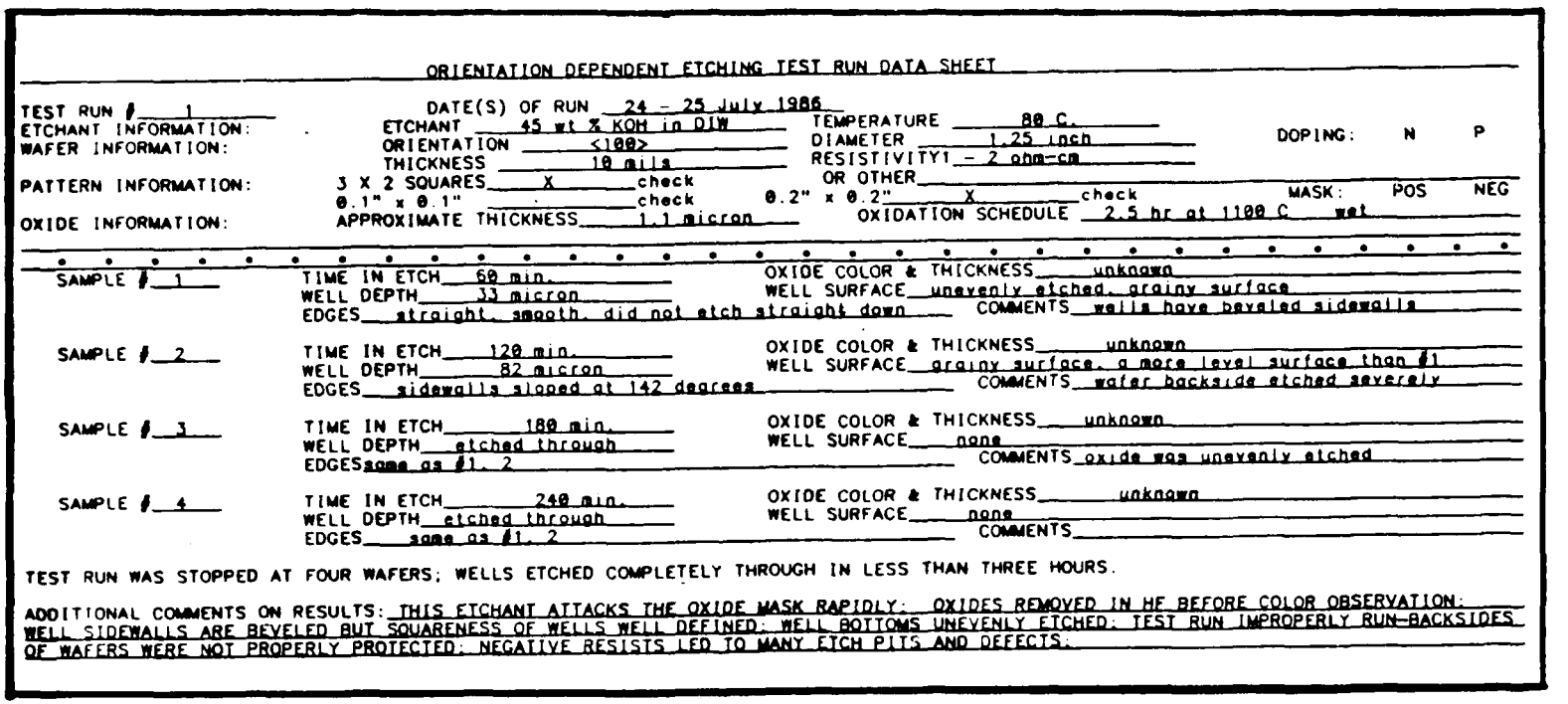
This cleaning solution is composed of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), and it is used to remove organic contaminants from the wafer's surface. These two components are mixed in a one to one proportion. The combination of these two constituent chemicals results in an exothermic reaction which generates a bubbling action. The reaction lasts only about 15 minutes, and the solution is fairly ineffective for cleaning wafers after that time.

This cleaning procedure is performed on the wafers prior to oxidation or whenever it is desired to have all organic contamination removed from the wafers. The procedure is:

1. Mix the 1:1 H_2SO_4:H_2O_2 solution in a clean glass beaker and immediately immerse the wafers for 15 minutes. The wafers can be placed in a polypropylene basket for convenient handling.
2. Rinse the wafers in deionized water (greater than 10 Megohms) for 5 minutes.
3. Dip the wafers in a 10:1 HF:Deionized water solution for 30 seconds. The hydrofluoric acid will remove an oxide glaze formed by step 1.
4. Rinse wafers in deionized water (greater than 10 Megohms) for 15 minutes.
5. Remove the wafers and blow dry with nitrogen gas.

Appendix E: Wet Orientation Dependent Etching Study Data (WODE) Sheets.

Figures E-1 to E-12 contain the data sheets for the WODE study. They are presented on the following pages.



ORIENTATION DEPENDENT ETCHING TEST RUN DATA SHEET

TEST RUN # 1 — DATE(S) OF RUN 24 - 25 July 1986

ETCHANT INFORMATION: ETCHANT 45 wt % KOH in DIW — TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> — DIAMETER 1.25 inch — DOPING: N P

THICKNESS 10 mils — RESISTIVITY1 - 2 ohm-cm

PATTERN INFORMATION: 3 X 2 SQUARES X check — OR OTHER — MASK: POS NEG

0.1" x 0.1" check — 0.2" x 0.2" X check

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 micron — OXIDATION SCHEDULE 2.5 hr at 1100 C wet

SAMPLE # 1 — TIME IN ETCH 60 min. — OXIDE COLOR & THICKNESS unknown
WELL DEPTH 33 micron — WELL SURFACE unevenly etched, grainy surface
EDGES straight, smooth, did not etch straight down — COMMENTS walls have beveled sidewalls

SAMPLE # 2 — TIME IN ETCH 120 min. — OXIDE COLOR & THICKNESS unknown
WELL DEPTH 82 micron — WELL SURFACE grainy surface, a more level surface than #1
EDGES sidewalls sloped at 142 degrees — COMMENTS wafer backside etched severely

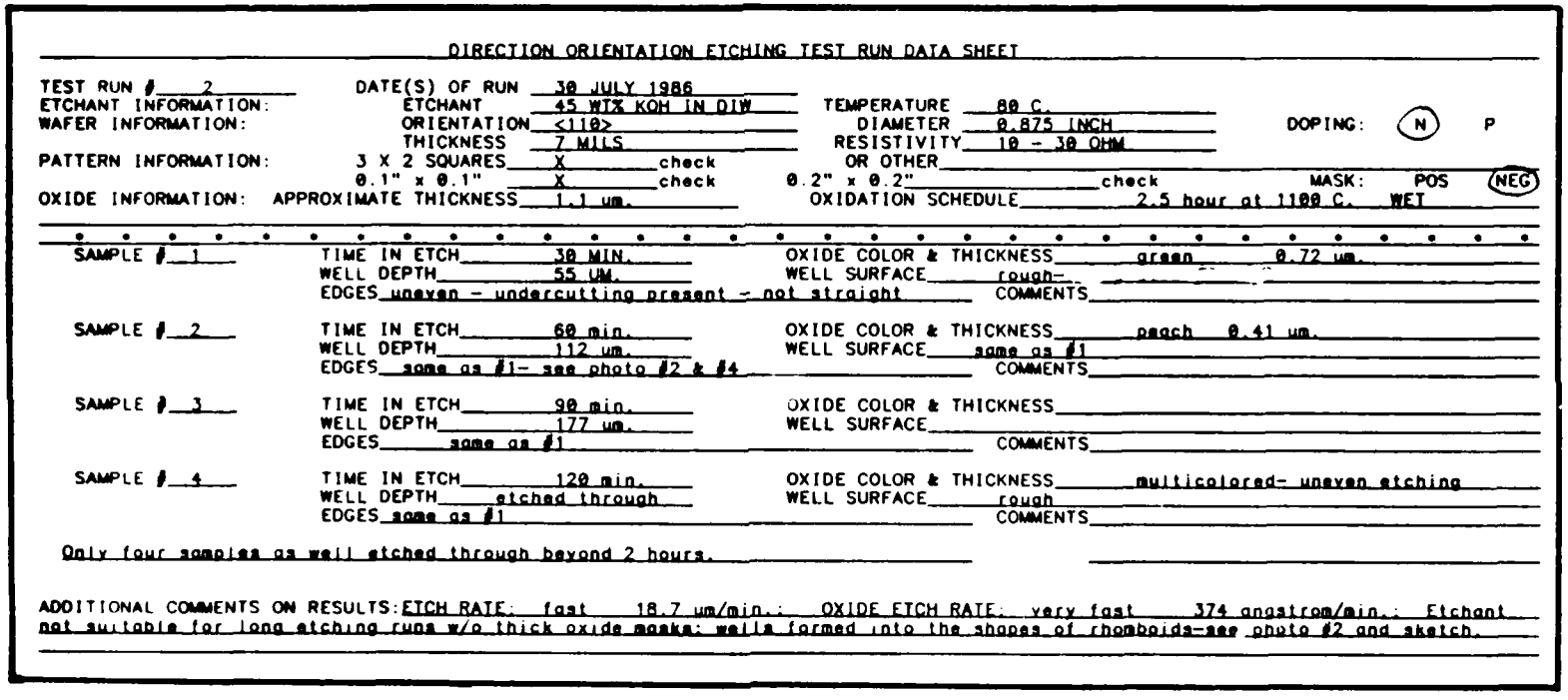
SAMPLE # 3 — TIME IN ETCH 180 min. — OXIDE COLOR & THICKNESS unknown
WELL DEPTH etched through — WELL SURFACE none
EDGES same as #1, 2 — COMMENTS oxide was unevenly etched

SAMPLE # 4 — TIME IN ETCH 240 min. — OXIDE COLOR & THICKNESS unknown
WELL DEPTH etched through — WELL SURFACE none
EDGES same as #1, 2 — COMMENTS

TEST RUN WAS STOPPED AT FOUR WAFERS; WELLS ETCHED COMPLETELY THROUGH IN LESS THAN THREE HOURS.

ADDITIONAL COMMENTS ON RESULTS: THIS ETCHANT ATTACKS THE OXIDE MASK RAPIDLY; OXIDES REMOVED IN HF BEFORE COLOR OBSERVATION; WELL SIDEWALLS ARE BEVELED BUT SQUARENESS OF WELLS WELL DEFINED; WELL BOTTOMS UNEVENLY ETCHED; TEST RUN IMPROPERLY RUN-BACKSIDES OF WAFERS WERE NOT PROPERLY PROTECTED; NEGATIVE RESISTS LED TO MANY ETCH PITS AND DEFECTS.

Figure E-1. Data Sheet - Wet Orientation Dependent Etching Study Trial # 1.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 2 DATE(S) OF RUN 30 JULY 1986

ETCHANT INFORMATION: ETCHANT 45 WT% KOH IN DIW TEMPERATURE 80 C

WAFER INFORMATION: ORIENTATION <110> DIAMETER 0.875 INCH DOPING: (N) P

THICKNESS 7 MILS RESISTIVITY 10 - 30 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" X check 0.2" x 0.2" check MASK: POS (NEG)

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 um. OXIDATION SCHEDULE 2.5 hour at 1100 C. WET

SAMPLE # 1
TIME IN ETCH 30 MIN. OXIDE COLOR & THICKNESS green 0.72 um.
WELL DEPTH 55 UM. WELL SURFACE rough-
EDGES uneven - undercutting present - not straight COMMENTS

SAMPLE # 2
TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS peach 0.41 um.
WELL DEPTH 112 um. WELL SURFACE same as #1
EDGES same as #1- see photo #2 & #4 COMMENTS

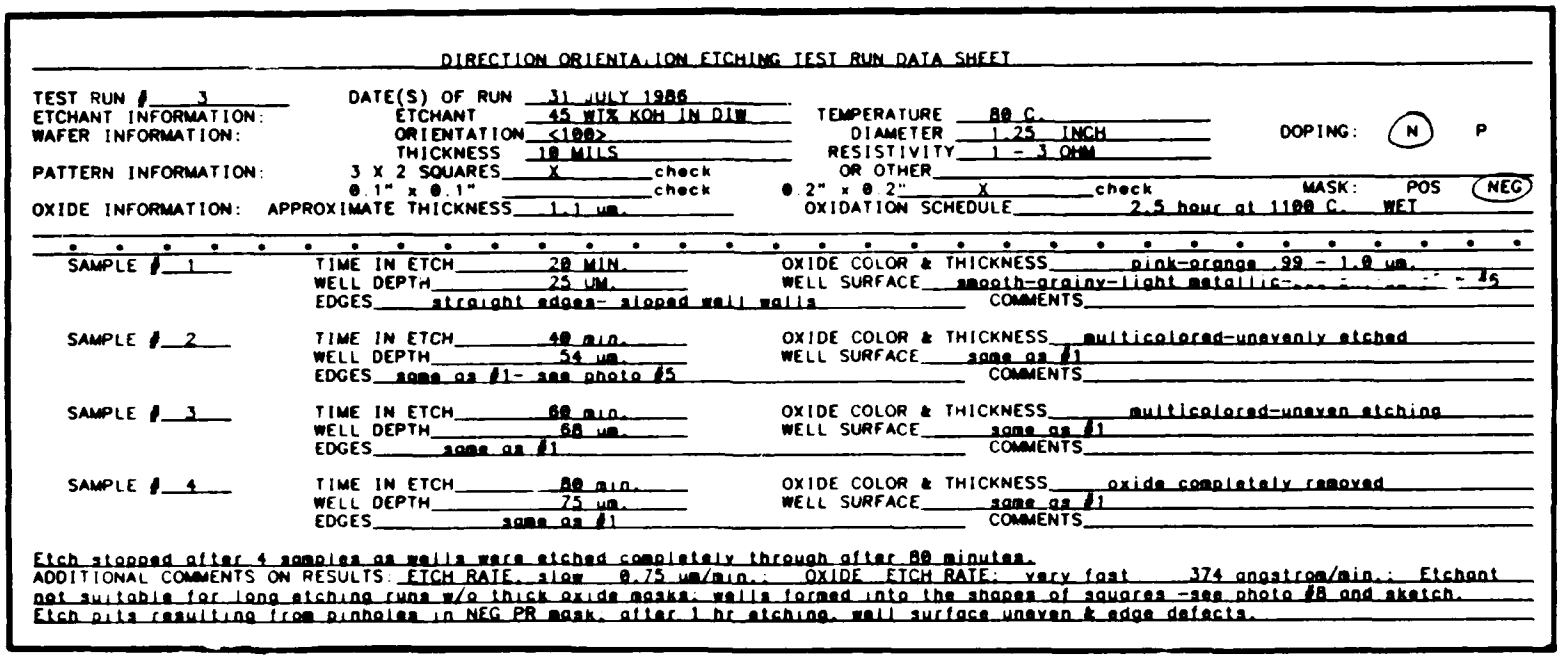
SAMPLE # 3
TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS
WELL DEPTH 177 um. WELL SURFACE
EDGES same as #1 COMMENTS

SAMPLE # 4
TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS multicolored- uneven etching
WELL DEPTH etched through WELL SURFACE rough
EDGES same as #1 COMMENTS

Only four samples as well etched through beyond 2 hours.

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: fast 18.7 um/min.; OXIDE ETCH RATE: very fast 374 angstrom/min.; Etchant not suitable for long etching runs w/o thick oxide masks; walls formed into the shapes of rhomboids-see photo #2 and sketch.

Figure E-2. Data Sheet - Wet Orientation Dependent Etching Study Trial # 2



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 3 DATE(S) OF RUN 31 JULY 1986

ETCHANT INFORMATION: ETCHANT 45 WT% KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER 1.25 INCH DOPING: (N) P

THICKNESS 10 MILS RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" check 0.2" x 0.2" X check MASK: POS (NEG)

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 um. OXIDATION SCHEDULE 2.5 hour at 1100 C. WET

SAMPLE # 1 TIME IN ETCH 20 MIN. OXIDE COLOR & THICKNESS pink-orange .99 - 1.0 um.

WELL DEPTH 25 UM. WELL SURFACE smooth-grainy-light metallic

EDGES straight edges- sloped wall walls COMMENTS

SAMPLE # 2 TIME IN ETCH 40 min. OXIDE COLOR & THICKNESS multicolored-unevenly etched

WELL DEPTH 54 um. WELL SURFACE same as #1

EDGES same as #1- see photo #5 COMMENTS

SAMPLE # 3 TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS multicolored-uneven etching

WELL DEPTH 68 um. WELL SURFACE same as #1

EDGES same as #1 COMMENTS

SAMPLE # 4 TIME IN ETCH 80 min. OXIDE COLOR & THICKNESS oxide completely removed

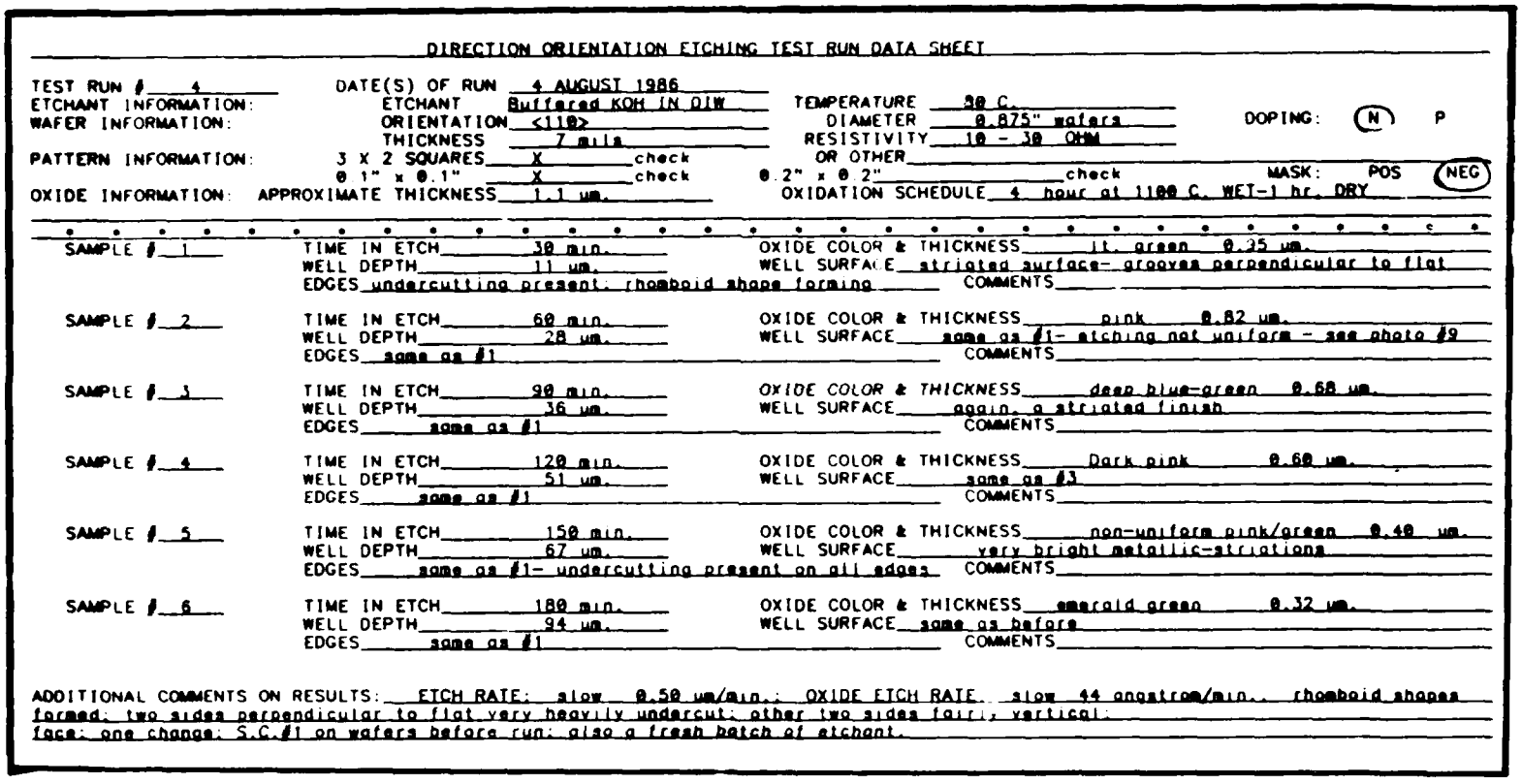
WELL DEPTH 75 um. WELL SURFACE same as #1

EDGES same as #1 COMMENTS

Etch stopped after 4 samples as walls were etched completely through after 80 minutes.

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE, slow 0.75 um/min.; OXIDE ETCH RATE: very fast 374 angstrom/min.; Etchant not suitable for long etching runs w/o thick oxide masks; walls formed into the shapes of squares -see photo #8 and sketch. Etch pits resulting from pinholes in NEG PR mask, after 1 hr etching, wall surface uneven & edge defects.

Figure E-3. Data Sheet - Wet Orientation Dependent Etching Study Trial #1



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 4 DATE(S) OF RUN 4 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH IN DIW TEMPERATURE 90 C.

WAFER INFORMATION: ORIENTATION <110> DIAMETER 0.875" wafers DOPING: (N) P

THICKNESS 7 mils RESISTIVITY 10 - 30 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" X check 0.2" x 0.2" check MASK: POS (NEG)

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 um. OXIDATION SCHEDULE 4 hour at 1100 C. WET-1 hr. DRY

SAMPLE # 1
TIME IN ETCH 30 min. OXIDE COLOR & THICKNESS lt. green 0.25 um.
WELL DEPTH 11 um. WELL SURFACE striated surface- grooves perpendicular to flat
EDGES undercutting present; rhomboid shape forming COMMENTS

SAMPLE # 2
TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS pink 0.82 um.
WELL DEPTH 28 um. WELL SURFACE same as #1- etching not uniform - see photo #9
EDGES same as #1 COMMENTS

SAMPLE # 3
TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS deep blue-green 0.68 um.
WELL DEPTH 36 um. WELL SURFACE again, a striated finish
EDGES same as #1 COMMENTS

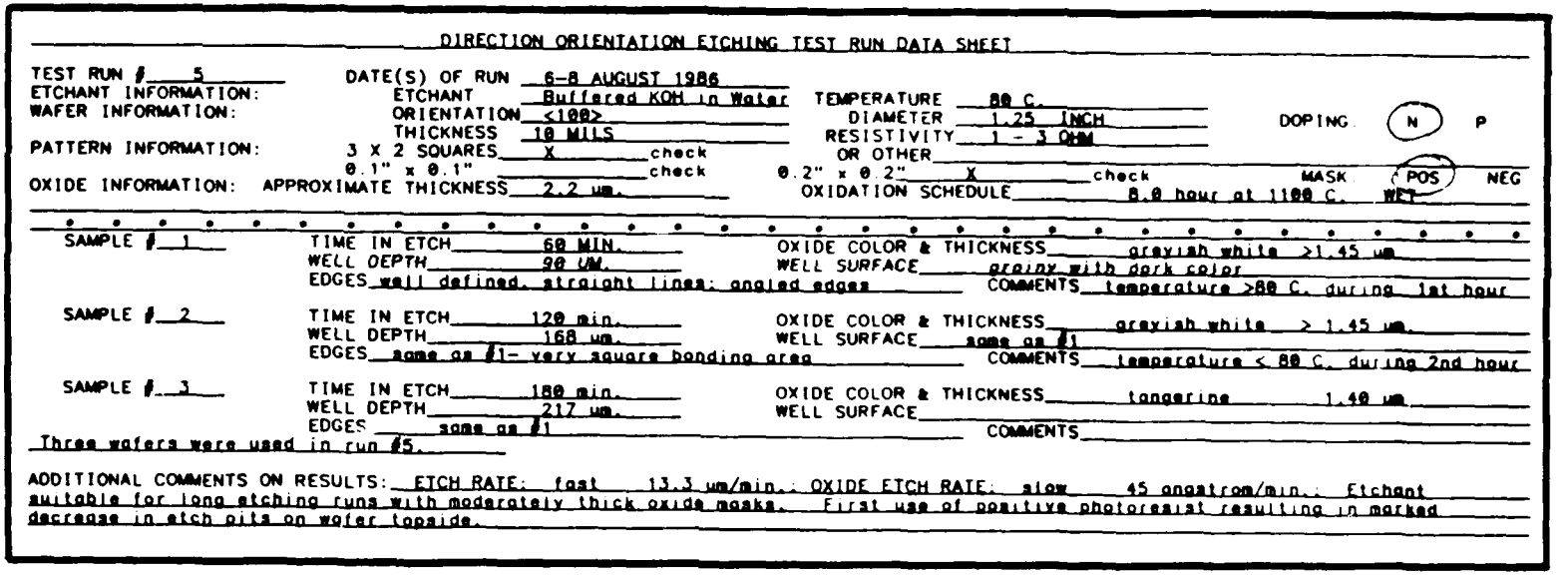
SAMPLE # 4
TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS Dark pink 0.60 um.
WELL DEPTH 51 um. WELL SURFACE same as #3
EDGES same as #1 COMMENTS

SAMPLE # 5
TIME IN ETCH 150 min. OXIDE COLOR & THICKNESS non-uniform pink/green 0.40 um.
WELL DEPTH 67 um. WELL SURFACE very bright metallic-striations
EDGES same as #1- undercutting present on all edges COMMENTS

SAMPLE # 6
TIME IN ETCH 180 min. OXIDE COLOR & THICKNESS emerald green 0.32 um.
WELL DEPTH 94 um. WELL SURFACE same as before
EDGES same as #1 COMMENTS

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: slow 0.50 um/min.; OXIDE ETCH RATE: slow 44 angstrom/min.; rhomboid shapes formed; two sides perpendicular to flat very heavily undercut; other two sides fairly vertical face; one change: S.C.#1 on wafers before run; also a fresh batch of etchant.

Figure E-4. Data Sheet - Wet Orientation Dependent Etching Study Trial # 4.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 5 DATE(S) OF RUN 6-8 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH in Water TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER 1.25 INCH DOPING (N) P

THICKNESS 10 MILS RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" check 0.2" x 0.2" X check MASK (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 2.2 um. OXIDATION SCHEDULE 8.0 hour at 1100 C. WET

SAMPLE # 1 TIME IN ETCH 60 MIN. OXIDE COLOR & THICKNESS greyish white >1.45 um

WELL DEPTH 90 UM. WELL SURFACE grainy with dark color

EDGES well defined, straight lines; angled edges COMMENTS temperature >80 C. during 1st hour

SAMPLE # 2 TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS greyish white > 1.45 um.

WELL DEPTH 168 um. WELL SURFACE same as #1

EDGES same as #1- very square bonding area COMMENTS temperature < 80 C. during 2nd hour

SAMPLE # 3 TIME IN ETCH 180 min. OXIDE COLOR & THICKNESS tangerine 1.40 um

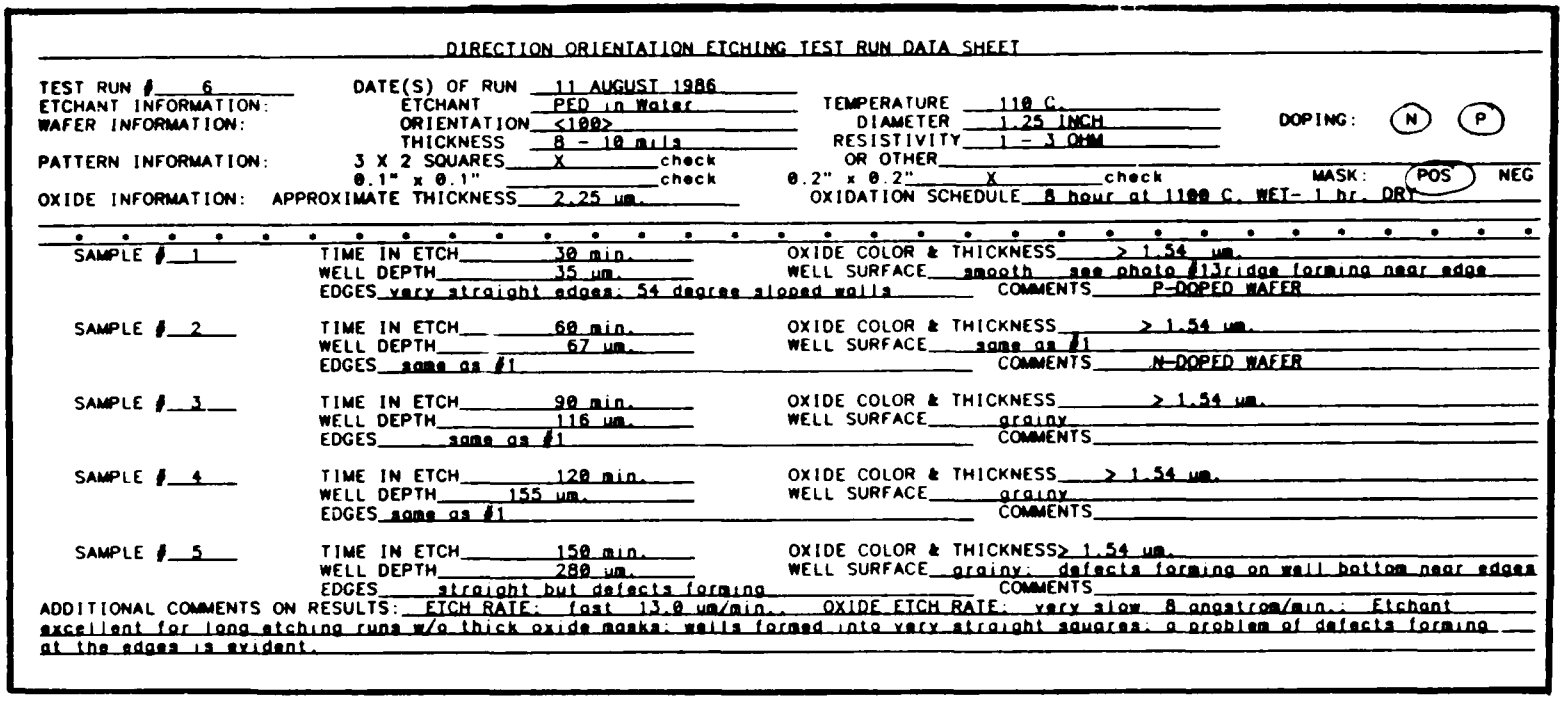
WELL DEPTH 217 um. WELL SURFACE

EDGES same as #1 COMMENTS

Three wafers were used in run #5.

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: fast 13.3 um/min.; OXIDE ETCH RATE: slow 45 angstrom/min.; Etchant suitable for long etching runs with moderately thick oxide masks. First use of positive photoresist resulting in marked decrease in etch pits on wafer topside.

Figure E-5. Data Sheet - Wet Orientation Dependent Etching Study Trial # 5.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 6 DATE(S) OF RUN 11 AUGUST 1986

ETCHANT INFORMATION: ETCHANT PED in Water TEMPERATURE 110 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER 1.25 INCH DOPING: (N) (P)

THICKNESS 8 - 10 mils RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" check 0.2" x 0.2" X check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 2.25 um. OXIDATION SCHEDULE 8 hour at 1100 C. WET- 1 hr. DRY

SAMPLE # 1
TIME IN ETCH 30 min. OXIDE COLOR & THICKNESS > 1.54 um.
WELL DEPTH 35 um. WELL SURFACE smooth see photo #13 ridge forming near edge
EDGES very straight edges; 54 degree sloped walls COMMENTS P-DOPED WAFER

SAMPLE # 2
TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS > 1.54 um.
WELL DEPTH 67 um. WELL SURFACE same as #1
EDGES same as #1 COMMENTS N-DOPED WAFER

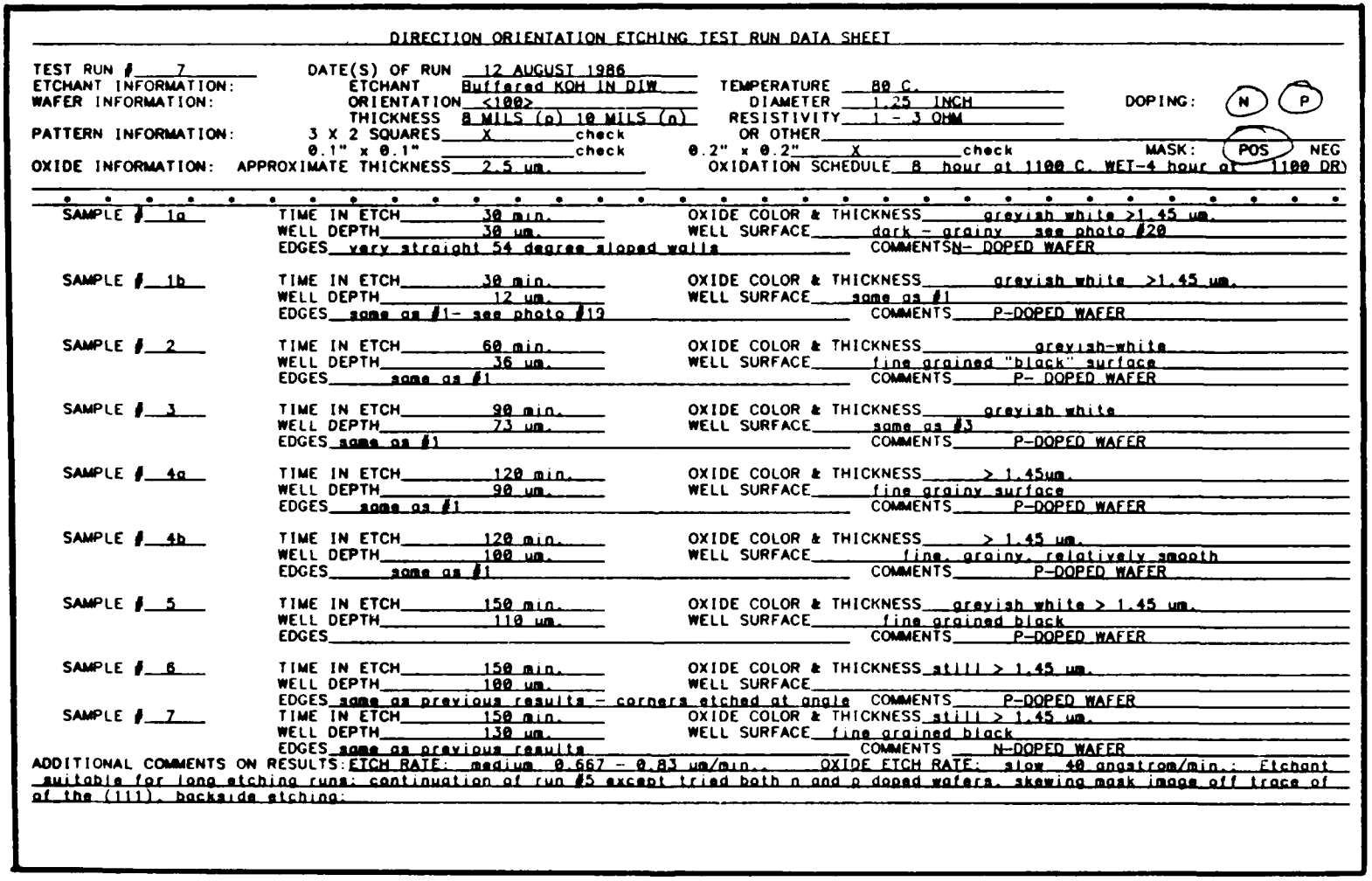
SAMPLE # 3
TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS > 1.54 um.
WELL DEPTH 116 um. WELL SURFACE grainy
EDGES same as #1 COMMENTS

SAMPLE # 4
TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS > 1.54 um.
WELL DEPTH 155 um. WELL SURFACE grainy
EDGES same as #1 COMMENTS

SAMPLE # 5
TIME IN ETCH 150 min. OXIDE COLOR & THICKNESS > 1.54 um.
WELL DEPTH 280 um. WELL SURFACE grainy; defects forming on well bottom near edges
EDGES straight but defects forming COMMENTS

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: fast 13.0 um/min.. OXIDE ETCH RATE: very slow 8 angstrom/min.; Etchant excellent for long etching runs w/o thick oxide masks; wells formed into very straight squares; a problem of defects forming at the edges is evident.

Figure E-6. Data Sheet - Wet Orientation Dependent Etching Study Trial # 6.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 7 DATE(S) OF RUN 12 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER 1.25 INCH DOPING: (N) (P)

THICKNESS 8 MILS (p) 10 MILS (n) RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" check 0.2" x 0.2" X check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 2.5 um. OXIDATION SCHEDULE 8 hour at 1100 C. WET-4 hour at 1100 DRY

SAMPLE # 1a TIME IN ETCH 30 min. OXIDE COLOR & THICKNESS greyish white >1.45 um.
WELL DEPTH 30 um. WELL SURFACE dark - grainy see photo #20
EDGES very straight 54 degree sloped walls COMMENTS N- DOPED WAFER

SAMPLE # 1b TIME IN ETCH 30 min. OXIDE COLOR & THICKNESS greyish white >1.45 um.
WELL DEPTH 12 um. WELL SURFACE same as #1
EDGES same as #1- see photo #19 COMMENTS P-DOPED WAFER

SAMPLE # 2 TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS greyish-white
WELL DEPTH 36 um. WELL SURFACE fine grained "black" surface
EDGES same as #1 COMMENTS P- DOPED WAFER

SAMPLE # 3 TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS greyish white
WELL DEPTH 73 um. WELL SURFACE same as #3
EDGES same as #1 COMMENTS P-DOPED WAFER

SAMPLE # 4a TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS > 1.45um.
WELL DEPTH 90 um. WELL SURFACE fine grainy surface
EDGES same as #1 COMMENTS P-DOPED WAFER

SAMPLE # 4b TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS > 1.45 um.
WELL DEPTH 100 um. WELL SURFACE fine, grainy, relatively smooth
EDGES same as #1 COMMENTS P-DOPED WAFER

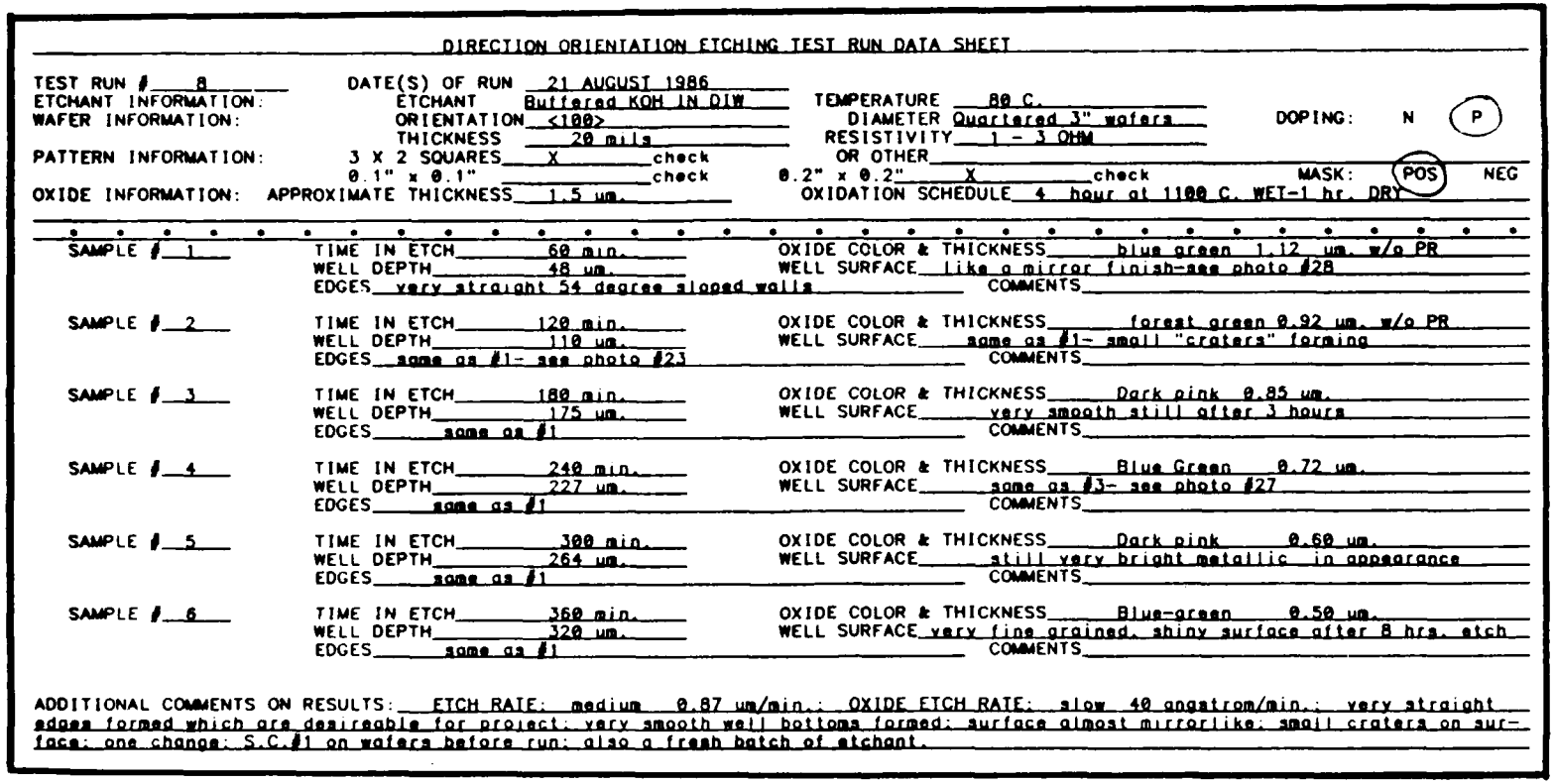
SAMPLE # 5 TIME IN ETCH 150 min. OXIDE COLOR & THICKNESS greyish white > 1.45 um.
WELL DEPTH 110 um. WELL SURFACE fine grained black
EDGES COMMENTS P-DOPED WAFER

SAMPLE # 6 TIME IN ETCH 150 min. OXIDE COLOR & THICKNESS still > 1.45 um.
WELL DEPTH 100 um. WELL SURFACE
EDGES same as previous results - corners etched at angle COMMENTS P-DOPED WAFER

SAMPLE # 7 TIME IN ETCH 150 min. OXIDE COLOR & THICKNESS still > 1.45 um.
WELL DEPTH 130 um. WELL SURFACE fine grained black
EDGES same as previous results COMMENTS N-DOPED WAFER

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.667 - 0.83 um/min. OXIDE ETCH RATE: slow 40 angstrom/min.: Etchant suitable for long etching runs; continuation of run #5 except tried both n and p doped wafers, skewing mask image off trace of of the (111), backside etching:

Figure E-7. Data Sheet - Wet Orientation Dependent Etching Study Trial # 7.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 8 DATE(S) OF RUN 21 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER Quartered 3" wafers DOPING: N (P)

THICKNESS 20 mils RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

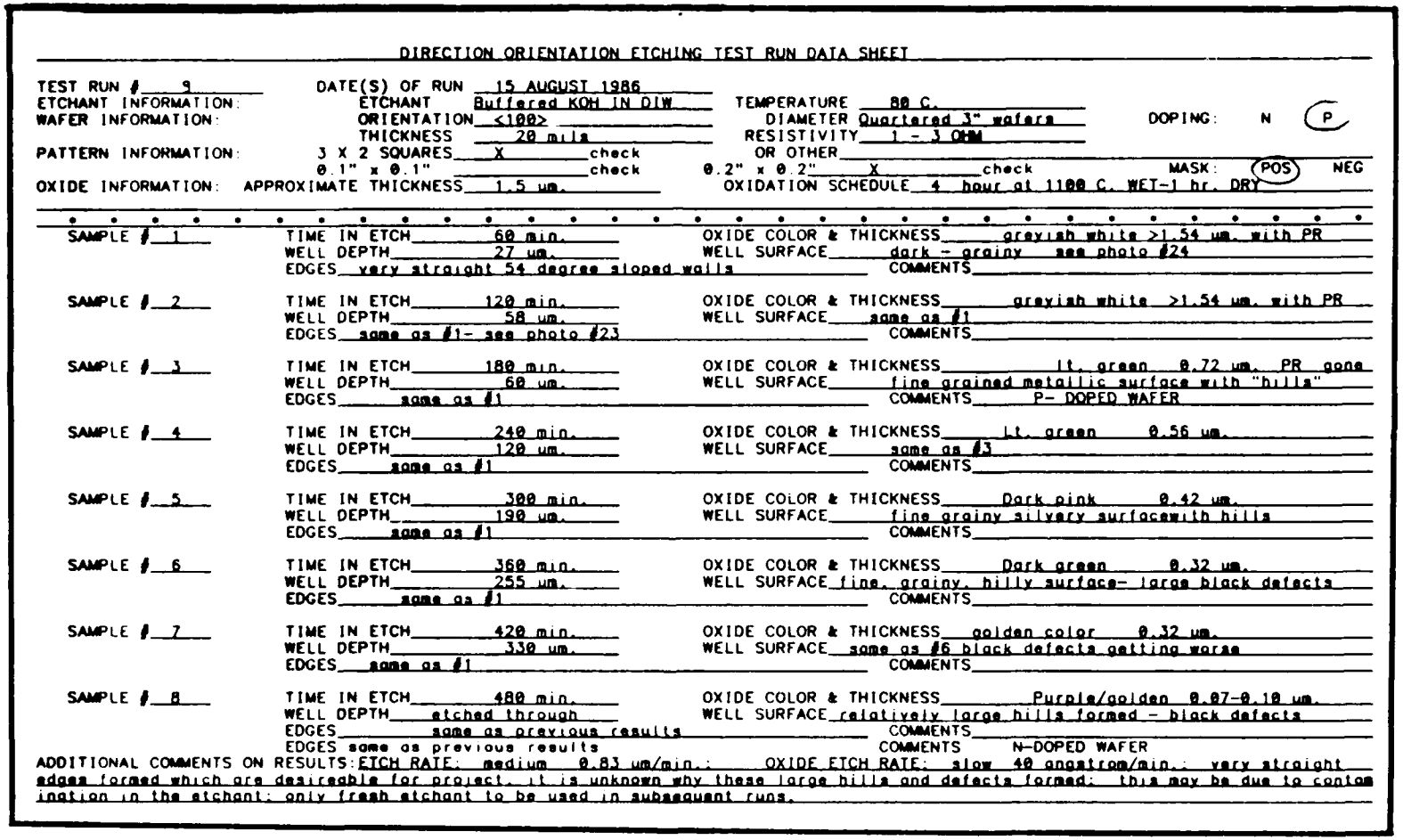
0.1" x 0.1" check 0.2" x 0.2" X check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.5 um. OXIDATION SCHEDULE 4 hour at 1100 C. WET-1 hr. DRY

SAMPLE # 1	TIME IN ETCH 60 min.	OXIDE COLOR & THICKNESS	blue green 1.12 um. w/o PR
	WELL DEPTH 48 um.	WELL SURFACE	like a mirror finish-see photo #28
	EDGES very straight 54 degree sloped walls	COMMENTS	
SAMPLE # 2	TIME IN ETCH 120 min.	OXIDE COLOR & THICKNESS	forest green 0.92 um. w/o PR
	WELL DEPTH 110 um.	WELL SURFACE	same as #1- small "craters" forming
	EDGES same as #1- see photo #23	COMMENTS	
SAMPLE # 3	TIME IN ETCH 180 min.	OXIDE COLOR & THICKNESS	Dark pink 0.85 um.
	WELL DEPTH 175 um.	WELL SURFACE	very smooth still after 3 hours
	EDGES same as #1	COMMENTS	
SAMPLE # 4	TIME IN ETCH 240 min.	OXIDE COLOR & THICKNESS	Blue Green 0.72 um.
	WELL DEPTH 227 um.	WELL SURFACE	same as #3- see photo #27
	EDGES same as #1	COMMENTS	
SAMPLE # 5	TIME IN ETCH 300 min.	OXIDE COLOR & THICKNESS	Dark pink 0.60 um.
	WELL DEPTH 264 um.	WELL SURFACE	still very bright metallic in appearance
	EDGES same as #1	COMMENTS	
SAMPLE # 6	TIME IN ETCH 360 min.	OXIDE COLOR & THICKNESS	Blue-green 0.50 um.
	WELL DEPTH 320 um.	WELL SURFACE	very fine grained, shiny surface after 8 hrs. etch
	EDGES same as #1	COMMENTS	

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.87 um/min.; OXIDE ETCH RATE: slow 40 angstrom/min.; very straight edges formed which are desireable for project; very smooth well bottoms formed; surface almost mirrorlike; small craters on surface; one change: S.C.#1 on wafers before run; also a fresh batch of etchant.

Figure E-8. Data Sheet - Wet Orientation Dependent Etching Study Trial # 8.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 9 DATE(S) OF RUN 15 AUGUST 1986

ETCHANT INFORMATION: ETCHANT Buffered KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <100> DIAMETER Quartered 3" wafers DOPING: N (P)

THICKNESS 20 mils RESISTIVITY 1 - 3 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

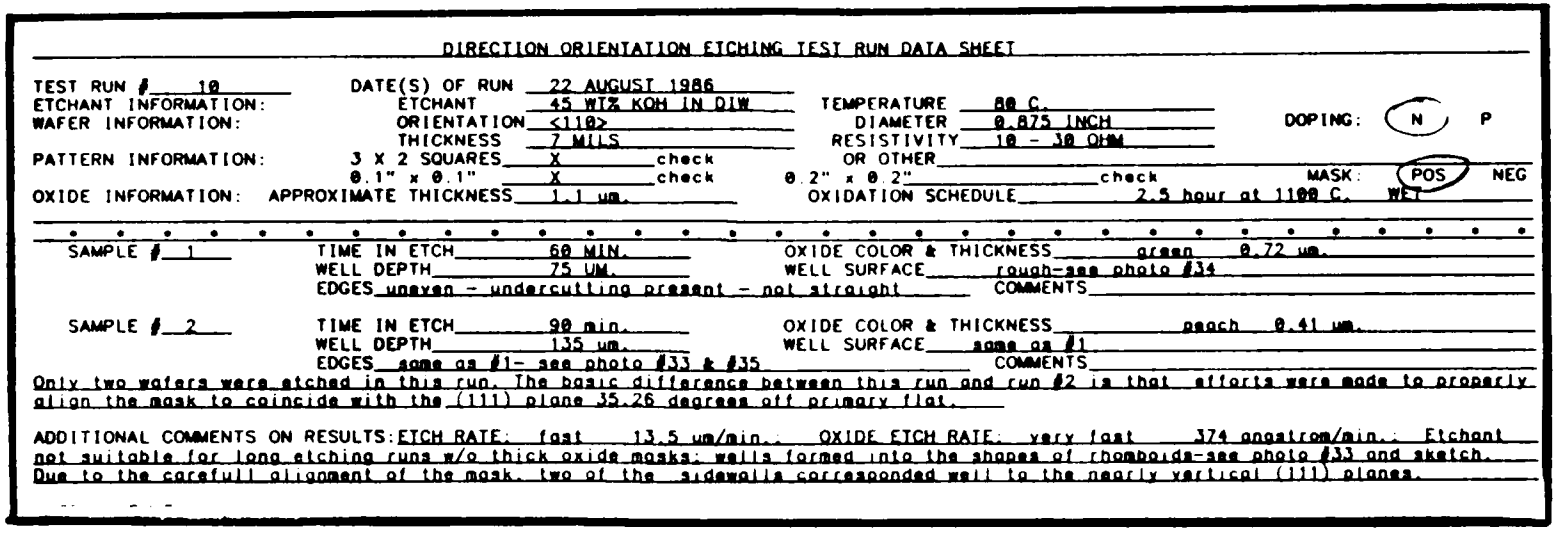
0.1" x 0.1" check 0.2" x 0.2" X check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.5 um. OXIDATION SCHEDULE 4 hour at 1100 C. WET-1 hr. DRY

SAMPLE # 1	TIME IN ETCH 60 min.	OXIDE COLOR & THICKNESS	greyish white >1.54 um. with PR
	WELL DEPTH 27 um.	WELL SURFACE	dark - grainy see photo #24
	EDGES very straight 54 degree sloped walls	COMMENTS	
SAMPLE # 2	TIME IN ETCH 120 min.	OXIDE COLOR & THICKNESS	greyish white >1.54 um. with PR
	WELL DEPTH 58 um.	WELL SURFACE	same as #1
	EDGES same as #1- see photo #23	COMMENTS	
SAMPLE # 3	TIME IN ETCH 180 min.	OXIDE COLOR & THICKNESS	lt. green 0.72 um. PR gone
	WELL DEPTH 60 um.	WELL SURFACE	fine grained metallic surface with "hills"
	EDGES same as #1	COMMENTS	P- DOPED WAFER
SAMPLE # 4	TIME IN ETCH 240 min.	OXIDE COLOR & THICKNESS	lt. green 0.56 um.
	WELL DEPTH 120 um.	WELL SURFACE	same as #3
	EDGES same as #1	COMMENTS	
SAMPLE # 5	TIME IN ETCH 300 min.	OXIDE COLOR & THICKNESS	Dark pink 0.42 um.
	WELL DEPTH 190 um.	WELL SURFACE	fine grainy silvery surfacewith hills
	EDGES same as #1	COMMENTS	
SAMPLE # 6	TIME IN ETCH 360 min.	OXIDE COLOR & THICKNESS	Dark green 0.32 um.
	WELL DEPTH 255 um.	WELL SURFACE	fine, grainy, hilly surface- large black defects
	EDGES same as #1	COMMENTS	
SAMPLE # 7	TIME IN ETCH 420 min.	OXIDE COLOR & THICKNESS	golden color 0.32 um.
	WELL DEPTH 330 um.	WELL SURFACE	same as #6 black defects getting worse
	EDGES same as #1	COMMENTS	
SAMPLE # 8	TIME IN ETCH 480 min.	OXIDE COLOR & THICKNESS	Purple/golden 0.07-0.10 um.
	WELL DEPTH etched through	WELL SURFACE	relatively large hills formed - black defects
	EDGES same as previous results	COMMENTS	
	EDGES same as previous results	COMMENTS	N-DOPED WAFER

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.83 um/min.; OXIDE ETCH RATE: slow 40 angstrom/min.; very straight edges formed which are desireable for project. It is unknown why these large hills and defects formed; this may be due to contamination in the etchant; only fresh etchant to be used in subsequent runs.

Figure E-9. Data Sheet - Wet Orientation Dependent Etching Study Trial # 9.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 10 DATE(S) OF RUN 22 AUGUST 1986

ETCHANT INFORMATION: ETCHANT 45 WT% KOH IN DIW TEMPERATURE 80 C.

WAFER INFORMATION: ORIENTATION <110> DIAMETER 0.875 INCH DOPING: (N) P

THICKNESS 7 MILS RESISTIVITY 10 - 30 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" X check 0.2" x 0.2" check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 um. OXIDATION SCHEDULE 2.5 hour at 1100 C. WET

SAMPLE # 1

TIME IN ETCH 60 MIN. OXIDE COLOR & THICKNESS green 0.72 um.

WELL DEPTH 75 UM. WELL SURFACE rough-see photo #34

EDGES uneven - undercutting present - not straight COMMENTS

SAMPLE # 2

TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS peach 0.41 um.

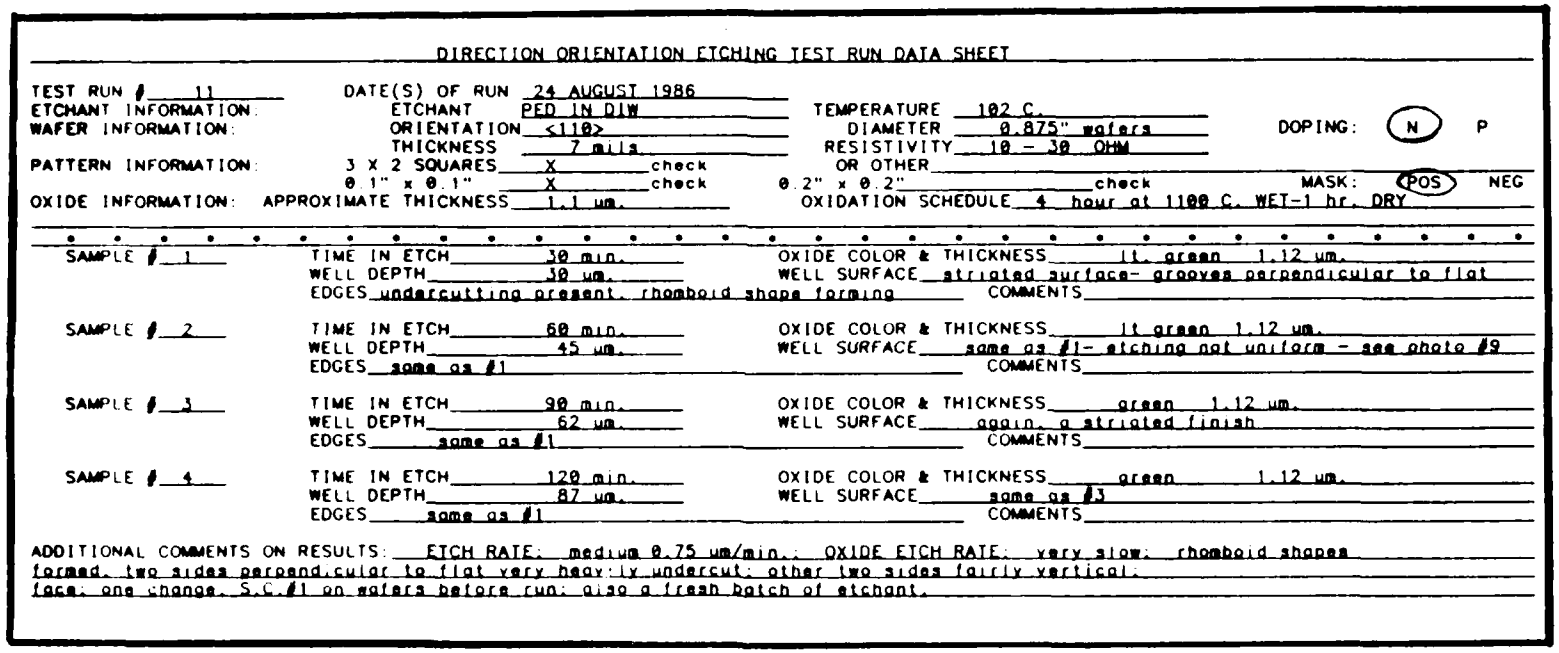
WELL DEPTH 135 um. WELL SURFACE same as #1

EDGES same as #1- see photo #33 & #35 COMMENTS

Only two wafers were etched in this run. The basic difference between this run and run #2 is that efforts were made to properly align the mask to coincide with the (111) plane 35.26 degrees off primary flat.

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: fast 13.5 um/min. OXIDE ETCH RATE: very fast 374 angstrom/min.: Etchant not suitable for long etching runs w/o thick oxide masks; walls formed into the shapes of rhomboids-see photo #33 and sketch. Due to the carefull alignment of the mask, two of the sidewalls corresponded well to the nearly vertical (111) planes.

Figure E-10. Data Sheet - Wet Orientation Dependent Etching Study Trial # 10.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 11 DATE(S) OF RUN 24 AUGUST 1986

ETCHANT INFORMATION: ETCHANT PED IN DIW TEMPERATURE 102 C.

WAFER INFORMATION: ORIENTATION <110> DIAMETER 0.875" wafers DOPING: (N) P

THICKNESS 7 mils RESISTIVITY 10 - 30 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check OR OTHER

0.1" x 0.1" X check 0.2" x 0.2" check MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 1.1 um. OXIDATION SCHEDULE 4 hour at 1100 C. WET-1 hr. DRY

SAMPLE # 1
TIME IN ETCH 30 min. OXIDE COLOR & THICKNESS lt. green 1.12 um.
WELL DEPTH 30 um. WELL SURFACE striated surface- grooves perpendicular to flat
EDGES undercutting present. rhomboid shape forming COMMENTS

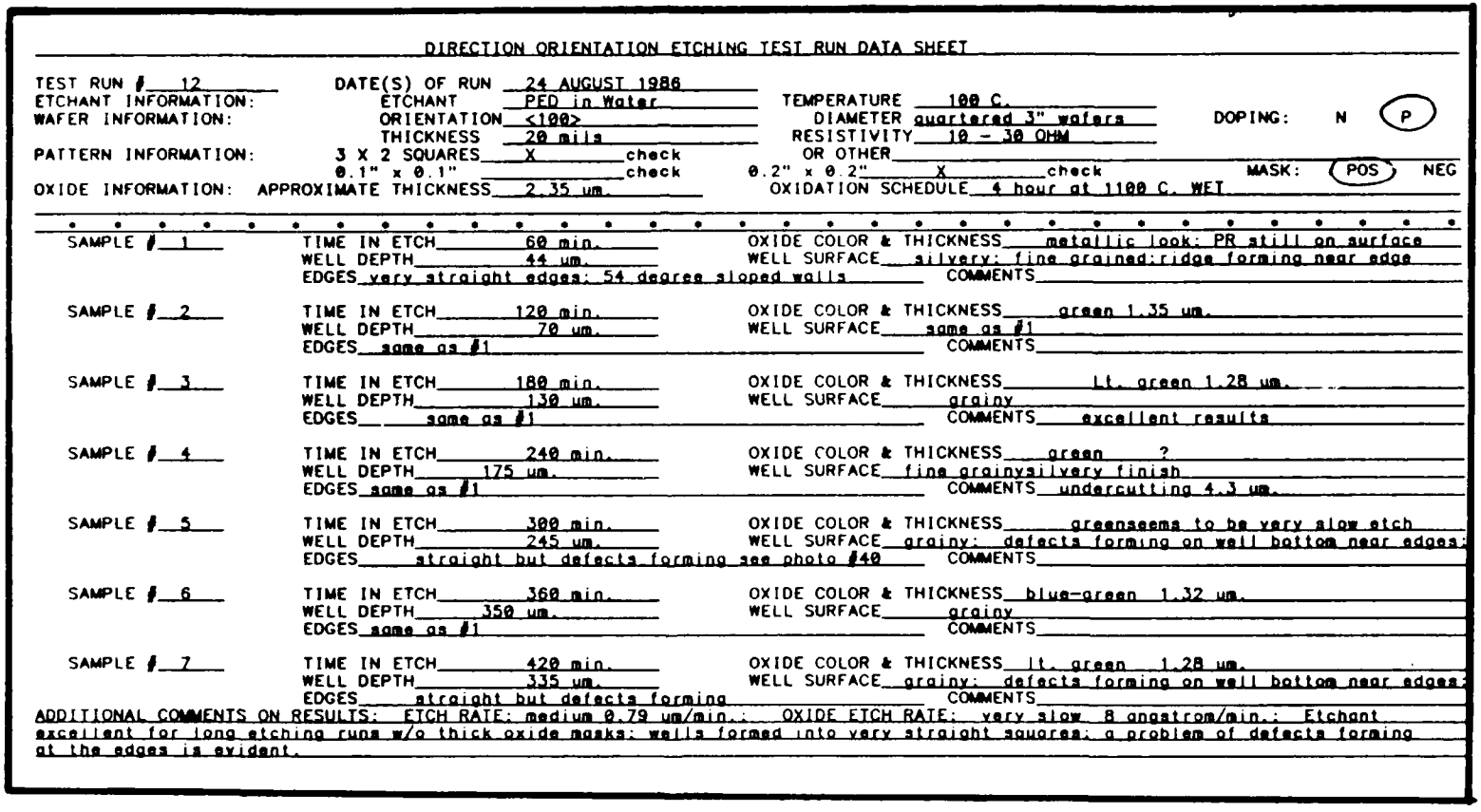
SAMPLE # 2
TIME IN ETCH 60 min. OXIDE COLOR & THICKNESS lt green 1.12 um.
WELL DEPTH 45 um. WELL SURFACE same as #1- etching not uniform - see photo #9
EDGES same as #1 COMMENTS

SAMPLE # 3
TIME IN ETCH 90 min. OXIDE COLOR & THICKNESS green 1.12 um.
WELL DEPTH 62 um. WELL SURFACE again, a striated finish
EDGES same as #1 COMMENTS

SAMPLE # 4
TIME IN ETCH 120 min. OXIDE COLOR & THICKNESS green 1.12 um.
WELL DEPTH 87 um. WELL SURFACE same as #3
EDGES same as #1 COMMENTS

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.75 um/min.; OXIDE ETCH RATE: very slow; rhomboid shapes formed, two sides perpendicular to flat very heavily undercut; other two sides fairly vertical face; one change, S.C.#1 on wafers before run; also a fresh batch of etchant.

Figure E-11. Data Sheet - Wet Orientation Dependent Etching Study Trial # 11.



DIRECTION ORIENTATION ETCHING TEST RUN DATA SHEET

TEST RUN # 12 — DATE(S) OF RUN 24 AUGUST 1986

ETCHANT INFORMATION: ETCHANT PED in Water — TEMPERATURE 100 C.

WAFER INFORMATION: ORIENTATION <100> — DIAMETER quartered 3" wafers — DOPING: N (P)

THICKNESS 20 mils — RESISTIVITY 10 - 30 OHM

PATTERN INFORMATION: 3 X 2 SQUARES X check — OR OTHER

0.1" x 0.1" check — 0.2" x 0.2" X check — MASK: (POS) NEG

OXIDE INFORMATION: APPROXIMATE THICKNESS 2.35 um. — OXIDATION SCHEDULE 4 hour at 1100 C. WET

SAMPLE # 1	TIME IN ETCH 60 min.	OXIDE COLOR & THICKNESS	metallic look: PR still on surface
	WELL DEPTH 44 um.	WELL SURFACE	silvery: fine grained:ridge forming near edge
	EDGES very straight edges: 54 degree sloped walls	COMMENTS	
SAMPLE # 2	TIME IN ETCH 120 min.	OXIDE COLOR & THICKNESS	green 1.35 um.
	WELL DEPTH 70 um.	WELL SURFACE	same as #1
	EDGES same as #1	COMMENTS	
SAMPLE # 3	TIME IN ETCH 180 min.	OXIDE COLOR & THICKNESS	lt. green 1.28 um.
	WELL DEPTH 130 um.	WELL SURFACE	grainy
	EDGES same as #1	COMMENTS	excellent results
SAMPLE # 4	TIME IN ETCH 240 min.	OXIDE COLOR & THICKNESS	green ?
	WELL DEPTH 175 um.	WELL SURFACE	fine grainysilvery finish
	EDGES same as #1	COMMENTS	undercutting 4.3 um.
SAMPLE # 5	TIME IN ETCH 300 min.	OXIDE COLOR & THICKNESS	greenseems to be very slow etch
	WELL DEPTH 245 um.	WELL SURFACE	grainy: defects forming on well bottom near edges:
	EDGES straight but defects forming see photo #40	COMMENTS	
SAMPLE # 6	TIME IN ETCH 360 min.	OXIDE COLOR & THICKNESS	blue-green 1.32 um.
	WELL DEPTH 350 um.	WELL SURFACE	grainy
	EDGES same as #1	COMMENTS	
SAMPLE # 7	TIME IN ETCH 420 min.	OXIDE COLOR & THICKNESS	lt. green 1.28 um.
	WELL DEPTH 335 um.	WELL SURFACE	grainy: defects forming on well bottom near edges:
	EDGES straight but defects forming	COMMENTS	

ADDITIONAL COMMENTS ON RESULTS: ETCH RATE: medium 0.79 um/min.; OXIDE ETCH RATE: very slow 8 angstrom/min.; Etchant excellent for long etching runs w/o thick oxide masks; wells formed into very straight squares; a problem of defects forming at the edges is evident.

Figure E-12. Data Sheet - Wet Orientation Dependent Etching Study Trial # 12.

Appendix F: Calibration of the Heat Block (Eutectic Material Bonding Procedure)

The temperature of the heat block was determined by the digital thermometer and thermocouple. To assure that the thermometer was registering the correct temperature, an experiment was performed to determine the correlation between the actual temperature and the measurements of the digital thermometer.

The principle behind the experiment was that five temperatures could be verified by observation and compared to the thermometer readings to determine the variance. The five temperatures are:

1. The temperature of ice water at 0 degrees Celsius.
2. The temperature of boiling water at 100 degrees Celsius.
3. The temperature of the melting point of a Gold-Tin preform at 276 degrees Celsius.
4. The temperature of the melting point of a Gold-Germanium preform at 325 degrees Celsius.
5. The temperature of the melting point of a Gold-Silicon preform at 356 degrees Celsius.

To verify the temperature at the freezing point, the heat block with the mounted thermocouple was placed in a liter of deonized water and ice. The temperature was recorded after the thermometer reading reached a steady state. To verify the temperature at the boiling point, the heat block was placed in a quartz vessel (one litre) and heated until boiling occured. The temperature was recorded after the thermometer reached a steady state. For the melting temperatures of the three eutectic preforms, the following procedure was used for each temperature. The heated on the hot plate just below the melting temperature (as read from the thermometer). One preform was

the heat block and the temperature was increased until the preform melted. The temperature was then recorded from the thermometer.

The results show that the accuracy of the digital thermometer decreases as higher temperature readings are taken. The readings at 0 degrees and 100 degrees Celsius were found to be very exact. The higher temperatures of the eutectic melting points were found to be much higher than expected. These temperatures are used in the eutectic material bonding procedure.

Appendix G: Metallization Process And Metal Etching Procedure.

Equipment and Materials. The following equipment was used in the metallization process and the metal etching procedure:

1. Aluminum Vacuum Evaporation System.
2. Custom wafer holders for quartered 3-inch wafers.
3. Beaker (200 ml made of pyrex).
4. Polyethylene wafer holder.
5. Pyrex thermometer.
6. Hot plate.

The following materials were used in the metallization and etch processes:

1. Aluminum wire.
2. Source boats.
3. Glacial Acetic Acid (CH_3COOH).
4. Phosphoric Acid (H_3PO_4).
5. Nitric Acid (HNO_3).

Procedure For Aluminum Evaporation. The fundamental procedures accomplished for evaporating the aluminum conductor thin-films were:

1. The wafer was purged with nitrogen gas to remove particulate matter.
2. The wafers and the aluminum source were mounted in the chamber, the chamber was evacuated, and aluminum was evaporated onto the polyimide's surface.
3. The aluminum film thickness was monitored with the Deposit Thickness Moniter meter (DTM-3, Sloan Instrument Corporation.

Santa Barbara, CA). When the desired film thickness was deposited, the chamber was vented, and the wafers were removed.

Procedure For The Aluminum Etch. The following procedure was used for the aluminum etch to etch the aluminum film into the desired conductor pattern:

1. The etchant solution was prepared by mixing the following constituents in a glass beaker: 20 milliliter (ml) nitric acid, 80 ml acetic acid, 80 ml phosphoric acid, and 20 ml deionized water were mixed as the etchant.
2. The etchant solution was heated to 45-50 degrees Celsius on a hot plate.
3. After the wafer was patterned with photoresist (See Chapter III), the wafer was immersed in the etchant.
4. The aluminum's etch rate was approximately 2000 angstroms/ minute. (The wafer must be carefully monitored to ensure complete removal in the desired areas.)
5. Finally, the photoresist was stripped from the wafer (for example, acetone was used to remove the positive resist).

Appendix H: The Digital Counter Circuitry.

Six digital counter circuits were designed and fabricated for the electrical evaluation of the final test samples. Details of the design are discussed below.

Design. A counter was used for each circuit under test. The purpose of the counter circuitry was to monitor the pulsed current passing through the circuit and recording the time into the test at which the circuit fails (if it fails at all). The mean-time-to-failure tests were planned to run for 60 hours with a pulsed current of 1 kHz passing through each circuit. The counter circuitry was designed to count a pulse by triggering on its leading edge. Obviously, if the test circuit's conductor fails (an open circuit), no signal will be measured by the counter.

Since the 60-hour test period is composed of 218,000 seconds, a 1kHz frequency pulse train implies that there will be 218×10^6 cycles. Thus, the counter will need to register a number of this magnitude. To achieve this goal, decade counters (SN74LS90) were utilized. The decade counter will count in binary output from 0 to 9 and then repeat. To obtain a pulse with which to trigger the next decade counter, the output of leads (Q_a and Q_d) were connected to a two-input NAND gate (7400 Quad Two-input NAND gates). Once (and only once) during the count from 0 to 9, the two leads Q_a and Q_d go to binary 1 or HIGH. The pulse from the NAND gate is binary 0 or LOW. This pulse was then inverted (7404 Hex Inverter). (Attempts to directly use AND gates failed for unknown reasons.) The

integration of these three digital circuits formed the fundamental stage in the counter design. This fundamental stage is illustrated in Figure H-1.

To obtain a counter capable of counting to 10^{10} as needed for the proposed test, ten of the fundamental stages were coupled together in series. The first stage receives the pulses coming directly from the signal generator through the circuit under test (as long as the circuit conducts). The pulses outputed from the first stage (and inputed to the second stage) have a 100 Hertz frequency. Accordingly, the output of the second stage has a 10 Hertz frquency, and the output of the third stage has a 1 Hertz frequency. The next seven stages count the 1 Hertz pulses. The last seven stages have light emitting diodes to facilitate observing the count status. With this counter circuit, a 1 millisecond count resolution is possible.

To properly calibrate the counter, an oscilloscope was connected to the counter and signal generator. The oscilloscope assured accurate timing because it provided a secondary means with which to assure that the frequency remained at 1 kHz. Calibration tests of the counter resulted in observations that were $\pm$ 0.01 % accurate.

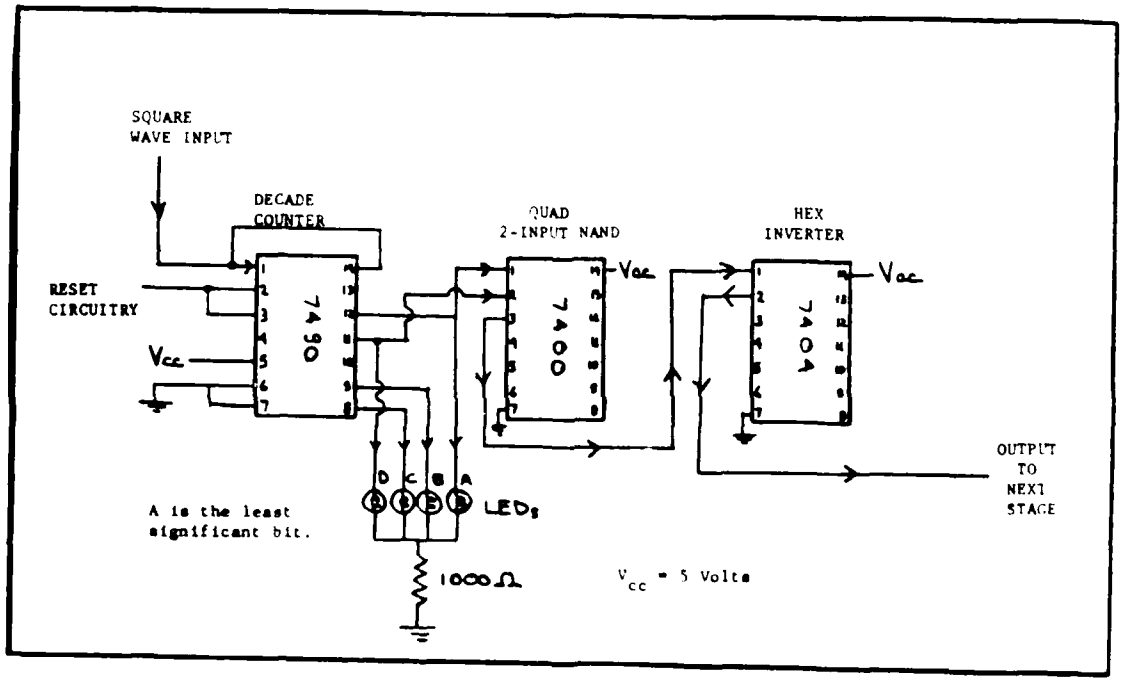


Figure H-1. Schematic of One Stage of the Digital Counter. Ten of these stages in series constitute a counter circuit capable of timing the mean-time-to-failure on a circuit tested for a duration as long as 60 hours with 1 millisecond accuracy.

Appendix I: Procedures For Applying Polyimide.

Equipment And Materials. The following equipment was used to applying the polyimide conformal coating:

1. Photoresist spinner,
2. Convection oven, and
3. Hot plate.

The following materials were used to apply the polyimide conformal coating:

1. Selectilux HTR 3-200 photosensitive polyimide precursor, 2. Selectiplast HTR AP-1 adhesion promoter, 3. Selectiplast D-2 developer,
4. Isopropyl alcohol, and
5. Mask alligner.

Application of the Polyimide. The following procedure was used to apply the polyimide conformal coating:

1. The wafer was baked at 150 degrees Celsius for 30 minutes to dehydrate the surface.
2. The adhesion promoter was mixed in a graduated cylinder as follows (two-day self life):
   a. 1-5 milliliter (ml) of HTR AP-1,
   b. 95 ml of isopropyl alcohol,
   c. 5 ml of DIW.
3. The wafer was removed from the oven and allowed to cool.
4. The wafer was placed on the photoresist spinner and the wafers were purged with nitrogen to remove particulate matter.

5. The wafer was flooded with the adhesion promoter for 10-15 seconds. The wafer was immediately spun on the photoresist spinner at 4000 rpm for 30 seconds.
6. The adhesion promoter was allowed to cure for 1 minute on the hot plate at 150 degrees Celsius.
7. The wafer was placed on the spinner and the wafers were purged with nitrogen to remove particulate matter.
8. The polyimide precursor was applied to the wafer with an eyedropper to cover approximately one-third of the wafer. The polyimide was spread on the wafer using a 20 second, 2000 rpm spin cycle (yields a 10 micron thick polyimide film after cure).
9. The wafer was softbaked at 65 degrees Celsius for 2 hours.
10. The wafer was removed from the oven and allowed to cool.

Exposing and Developing the Polyimide. To expose and develop the polyimide vias, the following procedure was implemented:

1. The wafers were purged with nitrogen gas to remove particulate matter.
2. The exposure level of the mask aligner was set to 400 mJ/cm^2. The mask was manually aligned with the wafer. The wafer was exposed to the ultraviolet light source.
3. The wafer was placed on the photoresist spinner. The wafer was spun at 500 rpm, and sprayed with the developer. After 25 seconds of spraying the developer, isopropyl alcohol was sprayed on the wafer as a rinse (5 second duration). The rinse was maintained for 15 seconds.

Curing the Polyimide. To cure the polyimide layer:

1. The oven was programmed as follows:

a. Hold 70 degrees Celsius,

b. S1 150 degrees Celsius for 1.5 hours,

c. S2 200 degrees Celsius for 1.5 hours,

d. S3 250 degrees Celsius for 4 hours.

2. The wafer was placed in the oven, and after approximately 7 hours, the wafer was removed

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VITA

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This study investigates a hybrid method of Wafer Scale Integration (WSI) which involves mounting discrete integrated circuit die into etched "wells" of a silicon wafer substrate, aligning the top surfaces of both the die and the silicon substrate, planarizing the gap between the die and the substrate, applying a conformal, dielectric smoothing layer, and finally, interconnecting the die utilizing a thin-film metallization conductor pattern. The study establishes a fabrication process by which functional integrated circuit die can be close-mounted and reliably interconnected with relatively low-loss conductors.

The study is composed of four phases. The first phase is the Wet Orientation Directed Etching (WODE) study which investigated the suitability of two silicon orientations and three etchants for creating the die "wells" in the support substrate. The second phase was the Die Attach Adhesive (DAA) study which investigated the performance of several hybrid circuit attachment adhesives for mounting the die in the "wells" of the substrate. The third phase involved the preparation of final samples for electrical performance evaluation. This phase utilized the results of the first two phases and involved a series of minor experiments which determined the optimum combinations of materials, techniques, and processing temperatures critical for achieving the final product. In the fourth phase, the evaluation of the electrical and thermal performance of the WSI samples was accomplished. In addition, the functional circuits were subjected to 60-hour, mean-time-to failure (MTTF) electrical tests at room temperature and 150 degrees Celsius. The surviving samples were then subjected to high temperature tests up to 350 degrees Celsius. After failure, each circuit was inspected to locate the failure. The early mortality percentage of the 54 circuits tested was 29.6 %. Three failures occurred after 60-hour tests at room temperature (5.6%); and three failures after the 60-hour test at 150 degrees Celsius (5.6%). Five of the remaining 40 circuits (9.3 %) failed when ramped to 350 degrees Celsius. Overall, 25 of 54 circuits (46.3%) survived all tests.

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